SNA
SENSE AND ACTUATE

SEM8310S

Ver 1.1

Aug. 21, 2014

SNA CO., LTD.

History

Ver 0.1	
Feb 8, 2012	1st version released
Ver 0.8	
Feb 10, 2012	Add BLCR Register and BLCR Register Write Enable bit in PMU
Ver 0.9	
Apr 4, 2012	Add EMB and Analog blocks
Ver 1.0	
Mar 15, 2013	Update ADC and EMB registers
Ver 1.1	
Aug 21, 2014	Fix EMB register addresses Rename Smart Metering(SEM8310) → SEM8310S

CONTENTS

FIGURES

TABLES

1 DESCRIPTIONS AND FEATURES

1.1 General Description

The SEM8310S is a 32-bit microcontroller with Serial Flash. It is a microcontroller that can operate up to 16MHz. The built-in Serial Flash is 512KB in size and includes 16KB SRAM.

The CPU is implemented independently of the bus for accessing program memory and data memory (Harvard architecture) and performs very fast instruction processing in EISC structure of 5-stage pipeline.

Serial Flash can be used for both program code and data, and JTAG programming method, which can be easily downloaded by users, is applied.

It also provides Idle mode and Deep Idle mode for low power applications.

1.2 Features

▫ High-performance, Low-power 32-bit EISC Microprocessor

▫ 32-bit EISC Architecture
- AE32000C
- DSP Extensions
- Loop Buffer
- Branch Prediction
- 2 Way 4Kbytes Instruction Cache
- JTAG Debugger
  - Core Debugger
  - Bus Debugger

▫ Program and Data Memories
- Serial Flash Memory Access
  - Using SPI Bus protocol Mode 3 and Mode 0
  - Support Single, Dual, Quad bit access
- 16KBytes Internal SRAM

▫ Peripherals
- 3 External Interrupts
- 18 Port In/Out with open drain mode
- AES-128
- Power Controller
- 32-bit Watchdog Timer
- 3 Channel 16-bit Timer/Counter with 15-bit Pre-scaler, Capture, PWM
- 3 Channel UART with 16Bytes FIFO, Functionally compatible with the 16550
- Master/Slave SPI with 8Bytes FIFO
- Two Wire Interface
- 2 x 2 Key Scan

- 32.768KHz crystal oscillator for RTC
- LCD Controller

▫ Special Features
- Program Security
  - ■ Copy Protection
- Power On Reset
- On-chip PLL
- LCD Driver
- Power Mode: Normal, Idle and Deep Idle mode

▫ Operating Voltage Range
- Core : 1.8V
- I/O : 3.3V

▫ Operating frequency
- Up to 16MHz

▫ Package
- 80-pin TQFP Package

2 BLOCK DIAGRAM & PIN DESCRIPTIONS

2.1 Block Diagram

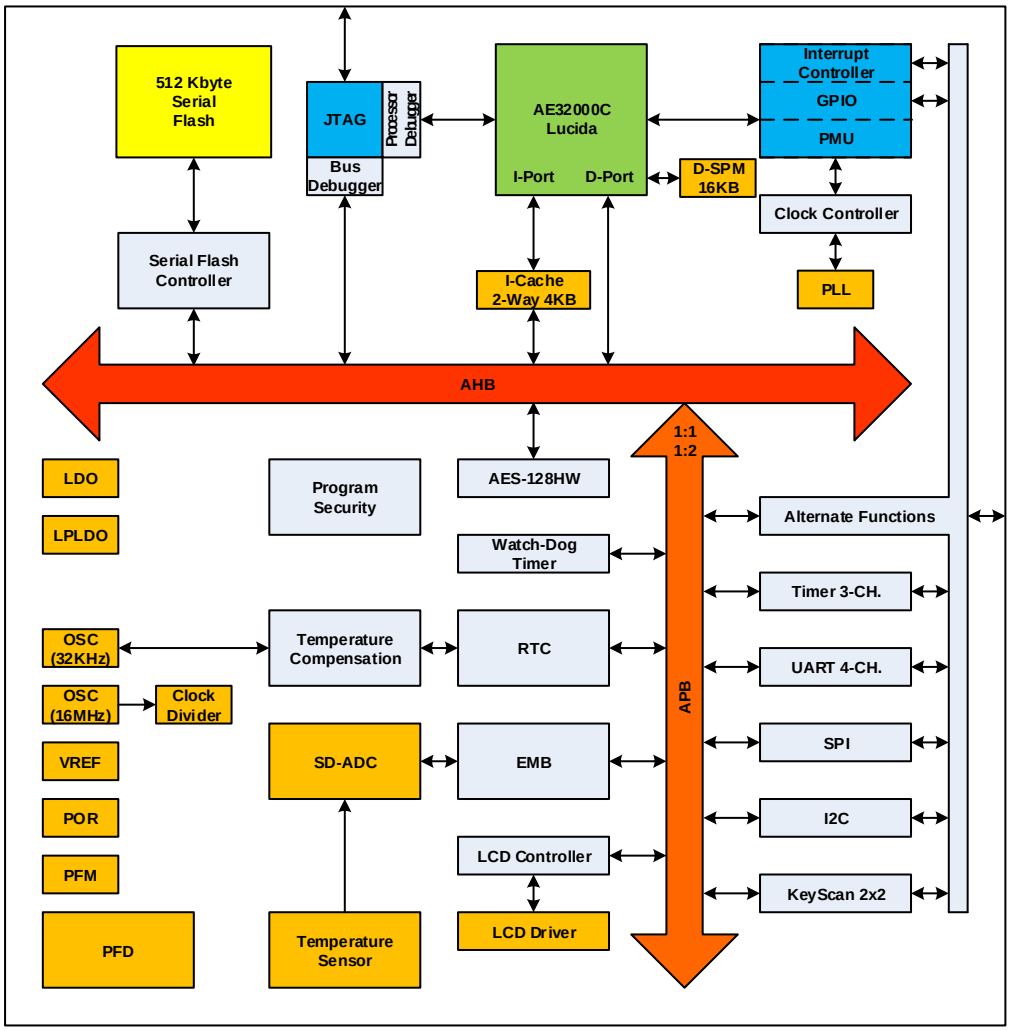


Figure 2-1 Block Diagram

2.2 Pin Configurations

Pinout

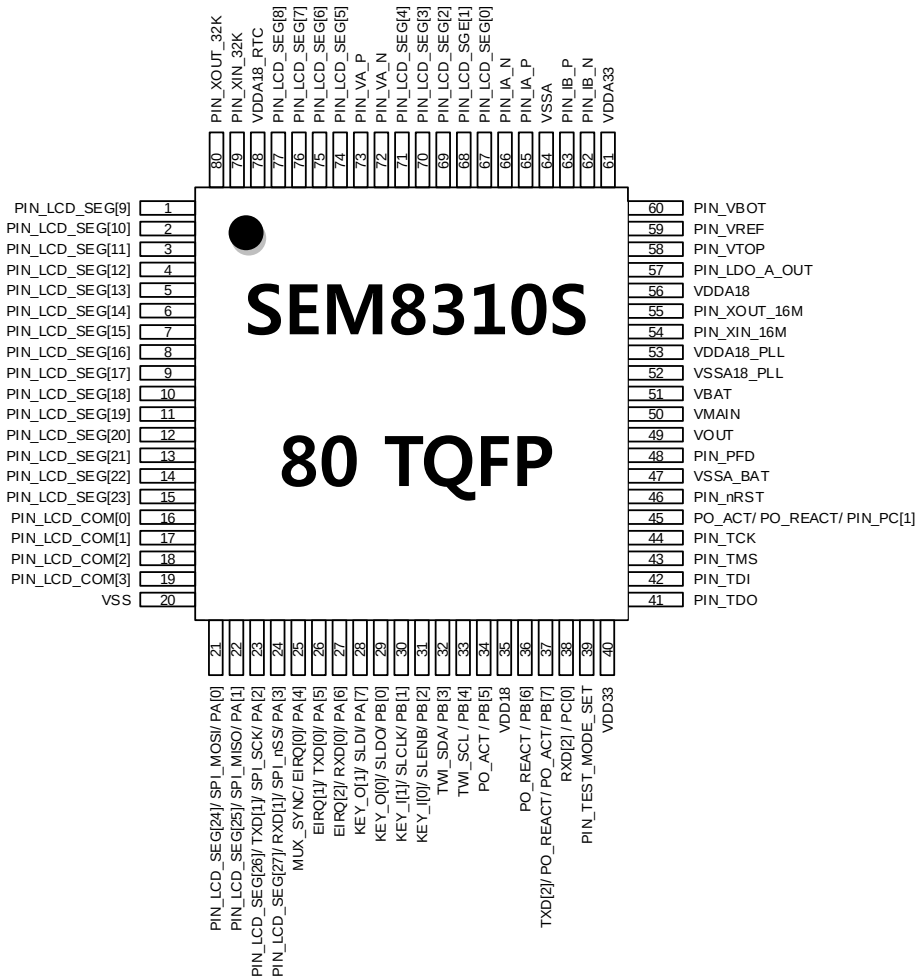


Figure 2-2 Pinout Diagram

Pin Definitions

Table 2.2-1 Pin Definitions

No.	*Name*	*Description*	*Type*	*Output Drive Current*	*Pull-Up/ Pull-Down*
1	PIN_LCD_SEG[9]	LCD Segment	Analog		
2	PIN_LCD_SEG[10]	LCD Segment	Analog		
3	PIN_LCD_SEG[11]	LCD Segment	Analog		
4	PIN_LCD_SEG[12]	LCD Segment	Analog		
5	PIN_LCD_SEG[13]	LCD Segment	Analog		
6	PIN_LCD_SEG[14]	LCD Segment	Analog		
7	PIN_LCD_SEG[15]	LCD Segment	Analog		
8	PIN_LCD_SEG[16]	LCD Segment	Analog		
9	PIN_LCD_SEG[17]	LCD Segment	Analog		
10	PIN_LCD_SEG[18]	LCD Segment	Analog		
11	PIN_LCD_SEG[19]	LCD Segment	Analog		
12	PIN_LCD_SEG[20]	LCD Segment	Analog		
13	PIN_LCD_SEG[21]	LCD Segment	Analog		
14	PIN_LCD_SEG[22]	LCD Segment	Analog		
15	PIN_LCD_SEG[23]	LCD Segment	Analog		
16	PIN_LCD_COM[0]	LCD Common	Analog		
17	PIN_LCD_COM[1]	LCD Common	Analog		
18	PIN_LCD_COM[2]	LCD Common	Analog		
19	PIN_LCD_COM[3]	LCD Common	Analog		
20	VSS				
21	PIN_LCD_SEG[24]/SPI_MOSI/PIN_PA[0]	LCD Segment SPI_MOSI GPIO A[0]	Analog In/Out In/Out		
22	PIN_LCD_SEG[25]/SPI_MISO/PIN_PA[1]	LCD Segment SPI_MISO GPIO A[1]	Analog In/Out In/Out		
23	PIN_LCD_SEG[26]/TXD[1]/SPI_SCK/PIN_PA[2]	LCD Segment Uart1 TXD SPI_SCK GPIO A[2]	Analog Out In/Out In/Out		
24	PIN_LCD_SEG[27]/RXD[1]/SPI_nSS/ PIN_PA[3]	LCD Segment Uart1 RXD SPI_nSS GPIO A[3]	Analog In In/Out In/Out		
25	MUX_SYNC/EIRQ[0]/PIN_PA[4]	External IRQ Source 0 GPIO A[4]	In In/Out		
26	EIRQ[1]/TXD[0]/PIN_PA[5]	External IRQ Source 1 Uart0 TXD GPIO A[5]	In Out In/Out		
27	EIRQ[2]/RXD[0]/PIN_PA[6]	External IRQ Source 2 Uart0 RXD GPIO A[6]	In In In/Out		
28	KEY_O[1]/SLDI/PIN_PA[7]	KeyScan1 Row GPIO A[7]	Out In/Out		
29	KEY_O[1]/SLDO/PIN_PB[0]	KeyScan0 Row GPIO B[0]	Out In/Out		
30	KEY_I[1]/SLCLK/PIN_PB[1]	KeyScan1 Colum GPIO B[1]	Out In/Out		

31	KEY_I[0]/SLENB/PIN_PB[2]	KeyScan0 Colum GPIO B[2]	In In/Out		
32	TWI_SDA/PIN_PB[3]	TWI SDA GPIO B[3]	IIn/Out In/Out		
33	TWI_SCL/PIN_PB[4]	TWI SCL GPIO B[4]	In/Out In/Out		
34	PO_ACT/PIN_PB[5]	Pulse Output GPIO B[5]	Out In/Out		
35	VDD18				
36	PO_REACT/PIN_PB[6]	Pulse Output GPIO B[6]	Out In/Out		
37	TXD[2]/PO_REACT/PO_ACT/PIN_PB[7]	Uart2 TXD Pulse Output GPIO B[7]	Out Out In/Out		
38	RXD[2]/PIN_PC[0]	Uart2 RXD GPIO C[0]	In In/Out		
39	PIN_TEST_MODE_SET	Test Mode Setting	In		
40	VDD33				
41	PIN_TDO	JTAG TDO	Out		
42	PIN_TDI	JTAG TDI	In		
43	PIN_TMS	JTAG TMS	In		
44	PIN_TCK	JTAG TCK	In		
45	PO_ACT/PO_REACT/PIN_PC[1]	Pulse Output GPIO C[1]	Out In/Out		
46	PIN_nRST	External Reset (Active low)	In		
47	VSSA_BAT				
48	PIN_PFD				
49	VOUT				
50	VMAIN				
51	VBAT				
52	VSSA18_PLL				
53	VDDA18_PLL				
54	PIN_XIN_16M	Input of 16MHz OSC			
55	PIN_XOUT_16M	Output of 16MHz OSC			
56	VDDA18				
57	PIN_LDO_A_OUT				
58	PIN_VTOP				
59	PIN_VREF				
60	PIN_VBOT				
61	VDDA33				
62	PIN_IB_N				
63	PIN_IB_P				
64	VSSA				
65	PIN_IA_P				
66	PIN_IA_N				
67	PIN_LCD_SEG[0]	LCD Segment			
68	PIN_LCD_SEG[1]	LCD Segment			
69	PIN_LCD_SEG[2]	LCD Segment			
70	PIN_LCD_SEG[3]	LCD Segment			
71	PIN_LCD_SEG[4]	LCD Segment			
72	PIN_VA_N				
73	PIN_VA_P				
74	PIN_LCD_SEG[5]	LCD Segment			
75	PIN_LCD_SEG[6]	LCD Segment			

76	PIN_LCD_SEG[7]	LCD Segment			
77	PIN_LCD_SEG[8]	LCD Segment			
78	VDDA18_RTC	VDDA18_RTC			
79	PIN_XIN_32K	Input of 32KHz OSC			
80	PIN_XOUT_32K	Output of 32KHz OSC			

Pin Descriptions

PIN_TEST_MODE_SET: Chip Test Mode Set

A dedicated pin, TEST_MODE_SET, determines the device operating mode. For normal operation, this pin should be kept at low level. If it is set to high level, it operates in Chip Test Mode.

In chip test mode, the following test mode is entered through the combination of the operation levels of TXD2 / PIN_PC [0], PIN_TMS, PIN_TDI and PIN_TDO 4 pins.

Mode		PIN_TEST_MODE_SET	RXD2/PIN_PC[0],	PIN_TMS	PIN_TDI	PIN_TDO
Normal Mode		0	x	x	x	x
MCU Test Mode		1	1	x	x	x
Test Mode	BIST	1	0	0	0	0
	SCAN	1	0	0	0	1
	PLL / LCD	1	0	0	1	0
	Analog Test	1	0	0	1	1

PO_ACT/PO_REACT/PIN_PC[1]:Power On Configuration

This pin is for selecting Debugger mode. This pin can be debugged by booting with a low level connection.

3 MEMORY ARCHITECTURE AND BOOTING MODE

3.1 Memory Map

The Memory Map is shown below..

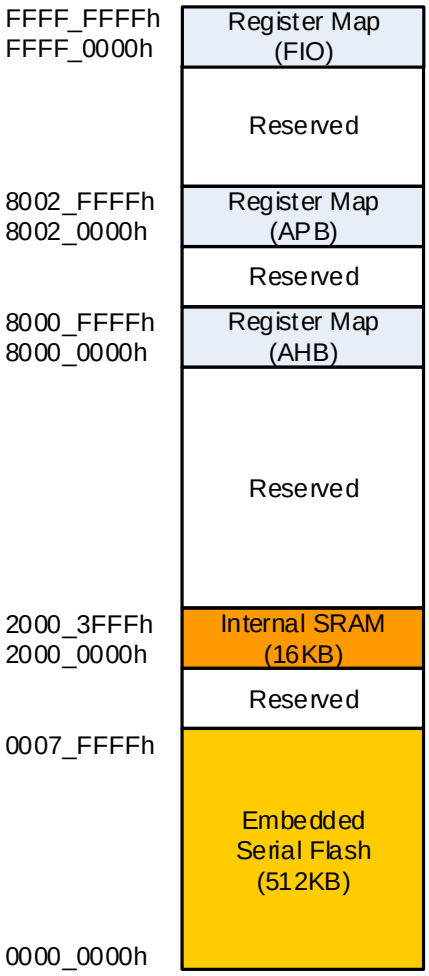


Figure 3-1 Memory Map

3.2 Embedded Memories

- 512KB Serial Flash
- 16KB SRAM
  - Single Cycle Access at full speed.

Serial Flash

512 KB Serial FLASH is built in. Can be used for commands or data.

Internal SRAM

There is a 16KB internal memory. Can be used for commands or data.

3.3 Memory Mapped I/O

The address of the Peripheral is as follows.

Table 3.3-1 Peripheral Memory Map

Base Address	*Offset Address*	*Block*
FIO 0xFFFF_0000	0x0000	Interrupt Controller
	0x1000	Reserved
	0x2000	Reserved
	0x3000	GPIO
	0x3000~FFFF	Reserved
AHB 0x8000_0000	0x0000	Serial Flash Controller
	0x0400	AES-128
	0x0800~0xFFFF	Reserved
APB 0x8002_0000	0x0000	Power Management Unit
	0x0400	Watch-Dog Timer
	0x0800	Timer
	0x0C00	UART
	0x1000	SPI
	0x1400	TWI
	0x1800	KeyScan
	0x1C00	Real Time Clock
	0x2000	EMB
	0x2400	LCD Controller
	0x2800	Reserved
	0x2C00	Reserved
	0x3000	Reserved
	0x3400	Reserved
	0x3800	Reserved
	0x3C00	Pin Alternate Function
	0x4000~0xFFFF	Reserved

3.4 Booting Configuration

Debugger Mode

Debugger mode is determined by the next pin.

PO_ACT / PO_REACT / PIN_PC [1]: Boots to Debugger mode when Low.

3.5 Copy Protection

Secure Mode

If you set the Secure bit (0x1) in the Copy Protection register (0x80000030), it will be in Secure mode.

When Copy Protection is set to Secure mode, the operation of Processor Debugger through JTAG is limited. Read / Program operation is restricted until Sector Erase when accessing Flash Memory to Bus Debugger. Sector erase of each sector of flash memory enables Read / Program operation only in the corresponding sector. If the Copy Protection register is set to Secure bit again, the subsequent operation is restricted. Also, in case of 0 sector in Secure mode, only Chip Erase operation is allowed.

With respect to Copy Protection, the Secure Flag registers that represent access restrictions to each sector are as follows.

0x80000030	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
	S7	S6	S5	S4	S3	S2	S1	Chip
	15bit	14bit	13bit	12bit	11bit	10bit	9bit	8bit
	S15	S14	S13	S12	S11	S10	S9	S8
	23bit	22bit	21bit	20bit	19bit	18bit	17bit	16bit
	S23	S22	S21	S20	S19	S18	S17	S16
	31bit	30bit	29bit	28bit	27bit	26bit	25bit	24bit
	S31	S30	S29	S28	S27	S26	S25	S24
0x80000034	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
	S39	S38	S37	S36	S35	S34	S33	S32
	15bit	14bit	13bit	12bit	11bit	10bit	9bit	8bit
	S47	S46	S45	S44	S43	S42	S41	S40
	23bit	22bit	21bit	20bit	19bit	18bit	17bit	16bit
	S55	S54	S53	S52	S51	S50	S49	S48
	31bit	30bit	29bit	28bit	27bit	26bit	25bit	24bit
	S63	S62	S61	S60	S59	S58	S57	S56
0x80000038	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
	S71	S70	S69	S68	S67	S66	S65	S64
	15bit	14bit	13bit	12bit	11bit	10bit	9bit	8bit
	S79	S78	S77	S76	S75	S74	S73	S72
	23bit	22bit	21bit	20bit	19bit	18bit	17bit	16bit
	S87	S86	S85	S84	S83	S82	S81	S80

	31bit	30bit	29bit	28bit	27bit	26bit	25bit	24bit
	S95	S94	S93	S92	S91	S90	S89	S88
0x8000003C	7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit
	S103	S102	S101	S100	S99	S98	S97	S96
	15bit	14bit	13bit	12bit	11bit	10bit	9bit	8bit
	S111	S110	S109	S108	S107	S106	S105	S104
	23bit	22bit	21bit	20bit	19bit	18bit	17bit	16bit
	S119	S118	S117	S116	S115	S114	S113	S112
	31bit	30bit	29bit	28bit	27bit	26bit	25bit	24bit
	S127	S126	S125	S124	S123	S122	S121	S120

If the Secure Flag of each sector in Flash Memory is '1', Read / Program operation is restricted
S1 to S127 are set to '0' for Sector Erase operation and Read / Program operation is allowed for the corresponding sector. 0bit of 0x80000030 indicates Secure Flag of all flash memory area. Only Chip Erase operation is allowed. When all flags are '0' after Chip Erase, Read / Program operation of all areas is allowed.

4 ANALOG BLOCKS

4.1 Introduction

The AFE (Analog Front End) of the SEM8310S consists of a 20-bit sigma-delta ADC, voltage reference, LDO, Voltage Monitor and Battery Manger.

4.2 Input Pins Configuration

The input pins of the AFE consist of differential current signal input pins such as IA_P / IA_N, IB_P / IB_N and differential voltage signal input pins such as VA_P / VA_N as shown in Figure 4-1. Here, the common of each pin is connected to the VREF pin of 0.9V.

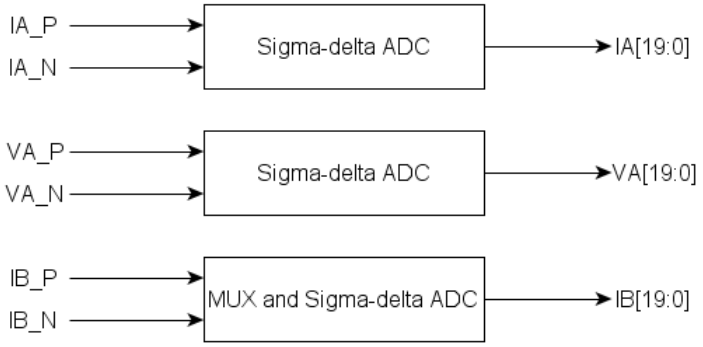


Figure 4-1 Configuration of AFE Input Pin and ADC

4.3 Analog to Digital Converter

The analog-to-digital converter (ADC) block of the AFE converts two currents and one voltage signal Input Pin (Differential) to a sigma-delta ADC, respectively, as shown in Figure 4-1. Here, the input signal is a voltage signal having a frequency band within 1.9 KHz and an amplitude within 500 mVpp (0.4 V to 1.4 V). All Sigma-delta ADCs have a Resolution of 20 bits and a Sampling Rate of 3,906.25 Hz, and their output data is stored in an EMB (Energy Measurement Block) register.

Table 4.3-1 ADC Register Configuration

Name	EMB Register Number	Bit	I/O
IA	0x8002_2008	32	I
VA	0x8002_200C	32	I
IB	0x8002_2010	32	I

4.4 Voltage Reference

The Voltage Reference generates three reference levels of 0.4V, 0.9V, and 1.4V for the ADC's high accuracy and is output via the VBOT and VREF, VTOP pins, respectively. VBOT, VREF, and VTOP pins are connected to external circuits consisting of capacitors (> 1uF) to suppress sampling noise and crosstalk from the ADC.

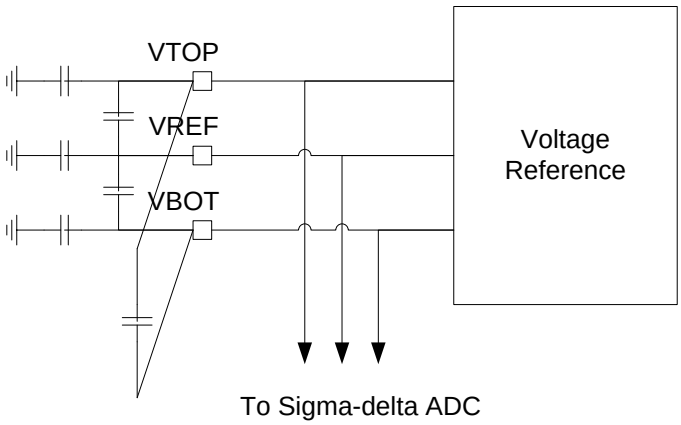


Figure 4-2 Configuration of Voltage Reference

4.5 Temperature Sensor

The temperature sensor senses the temperature of the on-chip and is used for temperature compensation for power metering information. The output of the temperature sensor is converted to digital data via a 20-bit ADC as shown in Figure 4-3 and stored in the EMB register. Here, the temperature sensing range is -40 ° C to 60 ° C and Resolution is within 5 ° C.

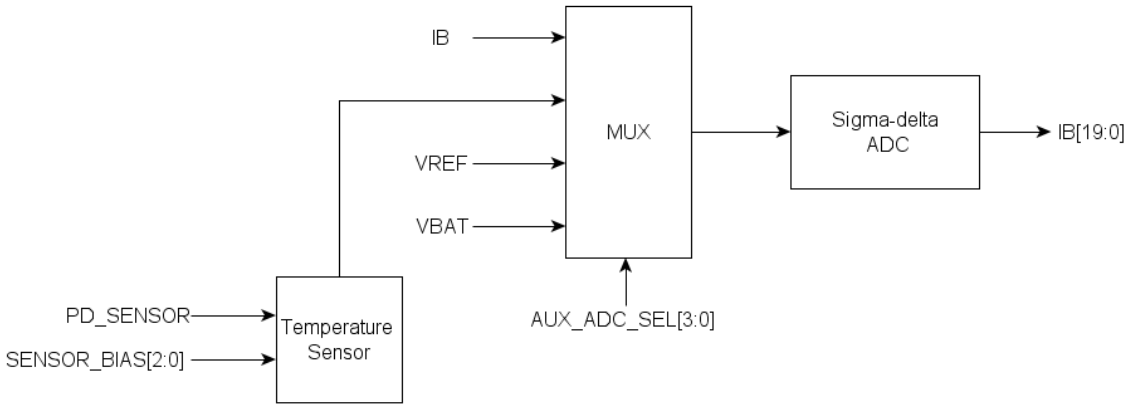


Figure 4- Configuration of Temperature and Voltage Monitor using 20bit ADC

Table 4.5-1 Register Configuration of 20bit ADC

AUX_ADC_SEL Register[3:0]	Output Data[19:0]
0001	IB
0010	Temperature Sensor
0100	VREF (=Offset)
1000	VBAT

4.6 Main Power Supply and Battery Voltage Monitor

The voltage of the main power supply (3.3V and 1.8V) and the battery (3.7V) are measured through a 20-bit ADC as shown in Figure 4-3 and stored in the EMB register.

Scale is adjusted to 1/2 of the input level of the channel and input to the ADC.

4.7 LDO

The LDO supplies 1.8V for Analog (VDDA18) and Digital (VDD18), ADC (VDDA18_ADC) and RTC (VDDA18_RTC) through the four pins LDO_OUT_A and LDO_OUT_D, LDO_OUT_ADC and LPLDO_OUT. Here, the RTC and the LDO for digital are automatically activated when 3.3V power is applied, and the LDO for analog and ADC are activated by the MCU through respective power-down registers.

4.8 Battery Manager

The battery manager detects whether the external main power is normal or brown-out and determines whether the battery is used according to the normal mode and the brownout mode of the system. Here, whether the external main power is normal is detected through the VPFD pin, and its threshold level can be adjusted by connecting a resistor to the VPFD pin.
The threshold level for failure detection of the external main power supply can be adjusted by the resistance ratio of R1 and R2 as shown in Table 4-4..

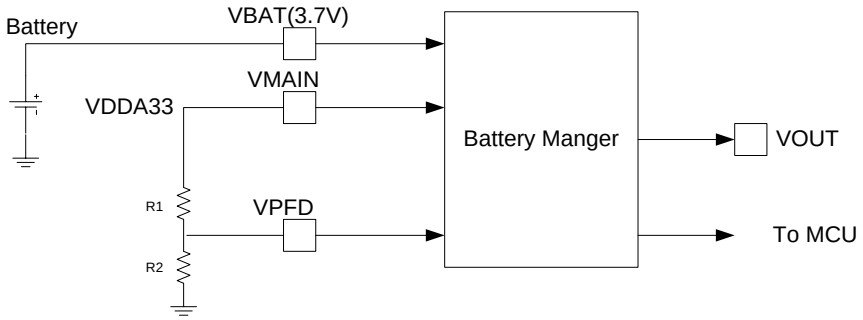


Figure 4-3 Battery Manager Configuration

Table 4.8-1 Threshold Voltage at VPFD pin to detect Power Failure

R1/R2 Ratio	Threshold Level [V]
0.7	2.55
0.8	2.7
0.9	2.85
1	3

5 CLOCKS AND POWER MANAGEMENT

5.1 Reset

The reset controller consists of Power On Reset, External Reset, Watch Dog Reset and Debugger Reset.

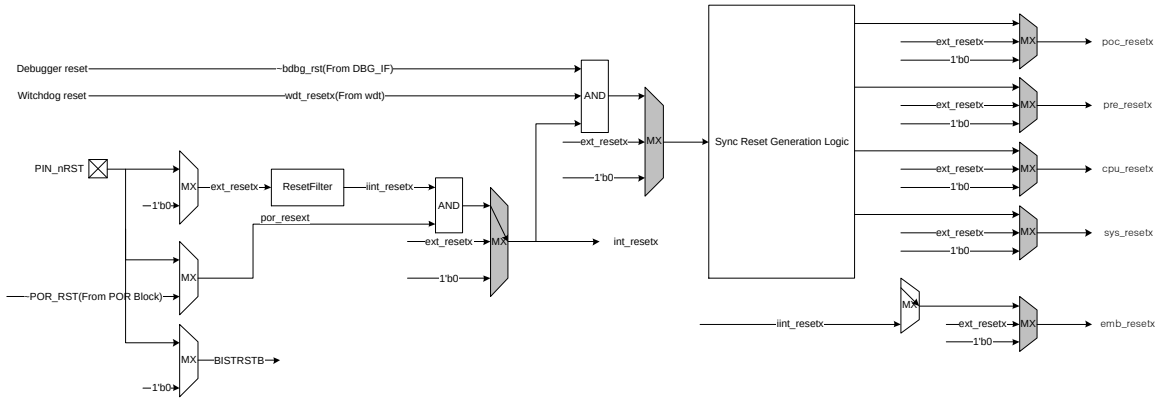


Figure 5-1 Reset Tree

Power On Start Time

Reset of POR is released and system reset is released after 1024-cycle based on XIN clock (16MHz).

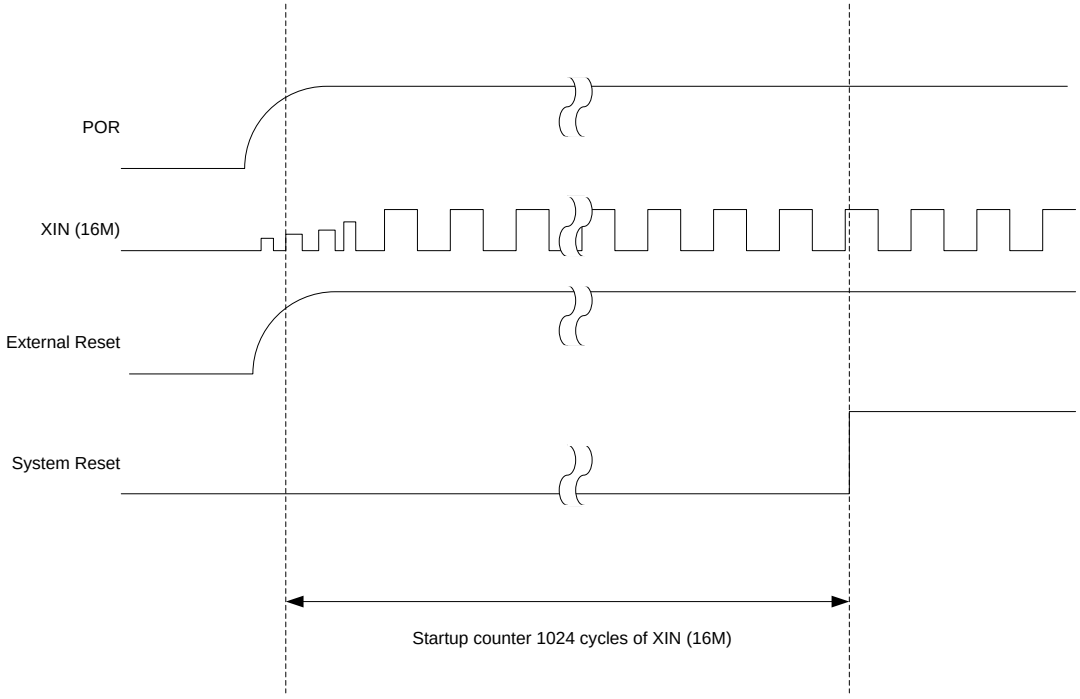


Figure 5-2 Power Up Reset

5.2 Clock

There are two external clock inputs and an internal PLL clock, and the structure is shown below.

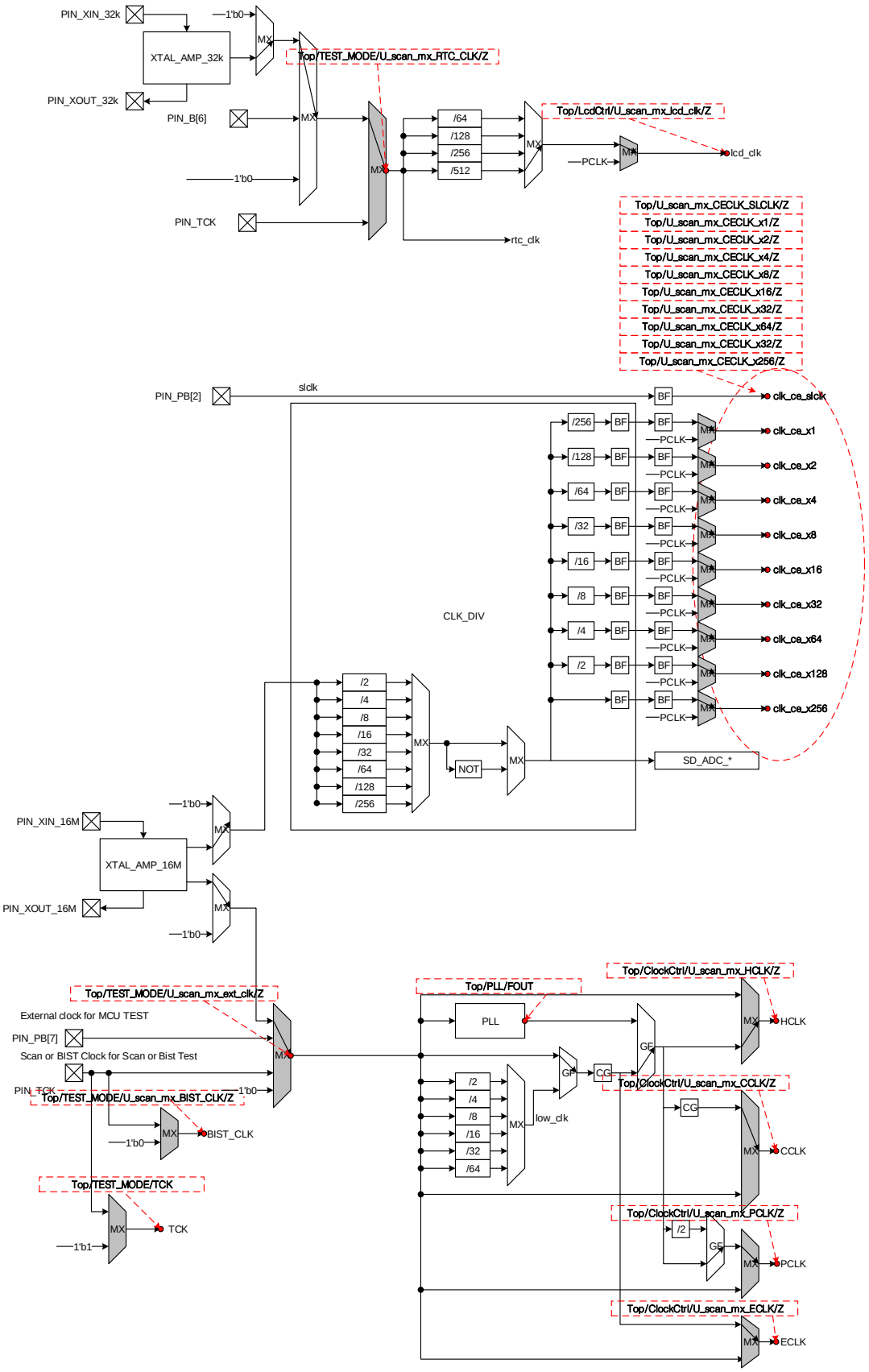


Figure 5-3 Clock Tree

OSC

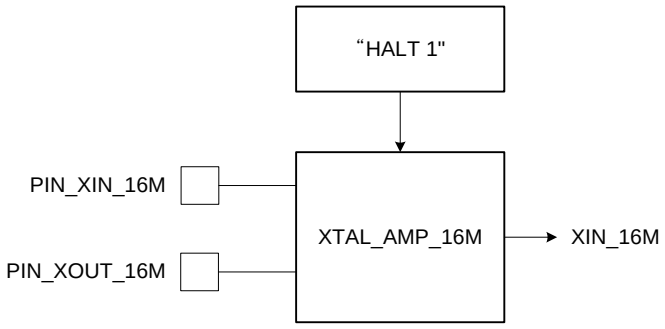


Figure 5-4 XTAL_AMP_16M Block Diagram

Figure 5-5 Typical Crystal Connection for XTAL_AMP_16M

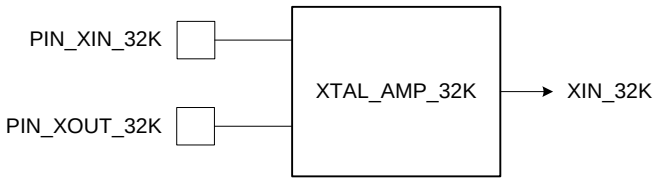


Figure 5-6 XTAL_AMP_32K Block Diagram

PLL

The internal PLL has a divider built in the input and output stages, so it has high precision.

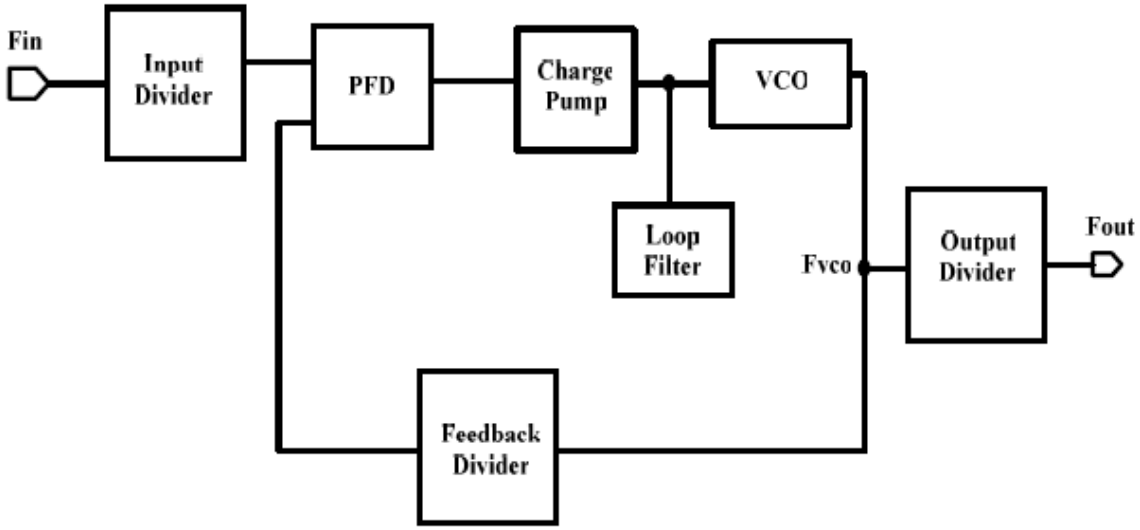


Figure 5-7 PLL Block Diagram

$$FOUT = \frac{FIN \times NF}{NR \times NO}$$

Where: FIN = 5 ~ 80MHz
FVCO = 200 ~ 400MHz
NR = Input Divider
NF = Feedback Divider
NO = Output Divider

To use the PLL, the PLLCTRL register must be controllable via the PLLWEN bit of the WENCTRL register. Then, the PLLCTRL register is controlled to set an appropriate clock to generate a PLL clock. After the lock time of the PLL, the system clock can be set to the PLL through the CLKCTRL register.

5.3 Power Management Controller

By setting the system clock, power consumption can be reduced. In addition to power consumption through clock setting, efficient power management can be achieved through power down of each analog and serial flash memory.

The following three power management modes are supported.

- Run Mode
- Idle Mode
- Deep Idle Mode

The figure below shows the transition between power modes.

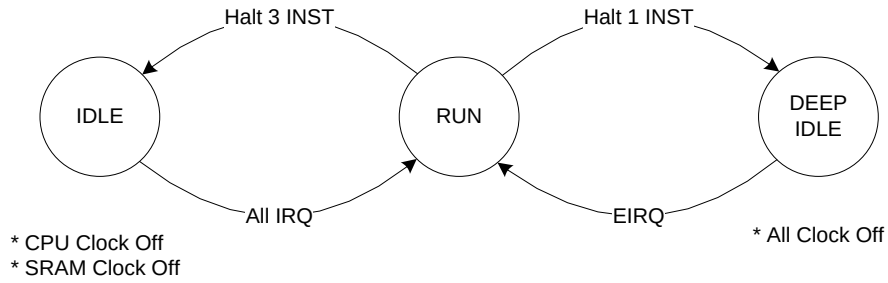


Figure 5-8 Power Mode State Diagram

Table 5.3-1 Power Mode

Power States	*Clocks*	*Wake-Up event*	*Description*
Run Mode	All Clock On		CPU Active
Idle Mode	CPU Clock Off	External Reset Watch Dog Reset All Interrupt	CPU Inactive Internal SRAM Inactive
Deep Idle Mode	All Clock Off	External Reset External Interrupt 0 External Interrupt 1 RTC_WIRQ ALL KEY IN	All Clock Off (Except RTC Clock)

Run Mode

CPU is processing instruction. In this mode, you can reduce the power consumption by lowering the frequency, and you can set it to operate directly by an external clock without using the PLL. Power down is possible if PLL is not used.

Idle Mode

The entry of Idle mode is done via the "Halt 3" command. In this mode, the clock supply of the CPU and internal SRAM is stopped and the CPU is stopped, but other peripherals can still operate.
The Wake-Up Source is as follows.

- External Reset
- Watch Dog Reset
- All Interrupt

Deep Idle Mode

Deep Idle mode is entered via the "Halt 1" command. In this mode, all clock supply is stopped and only the RTC clock is supplied.

Wake-Up Source는 is as follows.

- External Reset
- External Interrupt 0
- External Interrupt 1
- RTC IRQ
- ALL KEY Input

5.4 Power Management Control Registers

Write Enable Control Register (WENCTRL)

Address : 0x8002_0000

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
12	R/W	BLCR register enable bit 0 : Disable 1 : Enable	0
11	R/W	APDCTRL register enable bit 0 : Disable 1 : Enable	0
10	R/W	PLLCTRL register enable bit 0 : Disable 1 : Enable	0
9	R/W	LOWCTRL register enable bit 0 : Disable 1 : Enable	0
8	R/W	CLKCTRL register enable bit 0 : Disable 1 : Enable	0
7 : 3	R	Reserved	-
2	R/W	HALTCMD register enable bit 0 : Disable 1 : Enable	0
1 : 0	R	Reserved	-

*** To enter the power down mode via the HALT instruction, the HALTCMD register enable bit must be enabled.

Clock Control Register (CLKCTRL)

Address : 0x8002_0020

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	-
9	R/W	Wake-up for EIRQ1 level select bit 0 : Low level 1 : High level	0
8	R/W	Wake-up for EIRQ0 level select bit 0 : Low level 1 : High level	0
7	R/W	Wake-up for KEY enable bit 0 : Disable 1 : Enable	0
6	R/W	Wake-up for RTC enable bit 0 : Disable 1 : Enable	0
5	R/W	Wake-up for EIRQ1 enable bit 0 : Disable 1 : Enable	0
4	R/W	Wake-up for EIRQ0 enable bit 0 : Disable 1 : Enable	0
3	R	Reserved	-
2	R/W	PCLK clock selection 0 : HCLK 1 : HCLK / 2	0
1	R/W	HCLK clock selection 0 : External clock 1 : PLL clock	0
0	R/W	External clock selection 0 : XIN 1 : Low clock	0

*** This register is accessed by setting the Write Enable bit in the WENCTRL register to 1.

Low Control Register (LOWCTRL)

Address : 0x8002_0024

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
5 : 0	R/W	Low clock selection bit 000 : XIN / 2 001 : XIN / 4 010 : XIN / 8 011 : XIN / 16 100 : XIN / 32 101 : XIN / 64 11x : RTC clock	0

*** This register is accessed by setting the Write Enable bit in the WENCTRL register to 1.

PLL Control Register (PLLCTRL)

Address : 0x8002_0028

Bit	R/W	Description	Default Value
31 : 22	R	Reserved	-
21	R/W	RS : Reset signal (Active high) 0 : Disable 1 : Enable	1
20	R/W	PD : Power down (Active high) 0 : Disable 1 : Enable	1
19	R/W	OE : FOUT enable (Active low) 0 : Enable 1 : Disable	0
18	R/W	BP : Bypass the PLL (Active high) 0 : Disable 1 : Enable	0
17 : 16	R/W	O : Output divider	0
15 : 8	R/W	F : Feedback divider	0
7 : 6	R	Reserved	-
5	R/W	ID : Bypass input divider (Active high) 0 : Disable 1 : Enable	0
4 : 0	R/W	R : Reference divider	0

*** This register is accessed by setting the Write Enable bit in the WENCTRL register to 1.

Input Divider Value NR:

NR = R + 2

Feedback Divider Value NF:

NF = F + 2

Output Divider Value NO:

Output Divider Setting	NO (Output Divider Value)
00	1
01	2
10	2
11	4

$$FOUT = \frac{FIN \times NF}{NR \times NO}$$

Analog Power Down Control Register (APDCTRL)

Address : 0x8002_002C

Bit	R/W	Description	Default Value
15	RW	FILTER EN IB 0 : Disable 1 : Enable	0
14	RW	FILTER EN VA	0
13	RW	FILTER EN IA	0
12	RW	ADC PEN IB 0 : Disable 1 : Enable	0
11	RW	ADC CLK EN IB 0 : Disable 1 : Enable	0
10	RW	ADC PEN VA	0
9	RW	ADC CLK EN VA	0
8	RW	ADC PEN IA	0
7	RW	ADC CLK EN IA	0
6	RW	PD ADC VREFX 0 : Power ON 1 : Power Down	1
5	RW	PD SENSOR 0 : Power ON 1 : Power Down	1
4	RW	PD BOD 0 : Power ON 1 : Power Down	1
3	RW	Reserved	0
2	RW	ADC Filter Reset 0 : Reset 1 : Normal	0
1	RW	Clock Divider Reset 0 : Reset 1 : Normal	0
0	RW	EMB Reset 0 : Reset 1 : Normal	0

*** This register is accessed by setting the Write Enable bit in the WENCTRL register to 1.

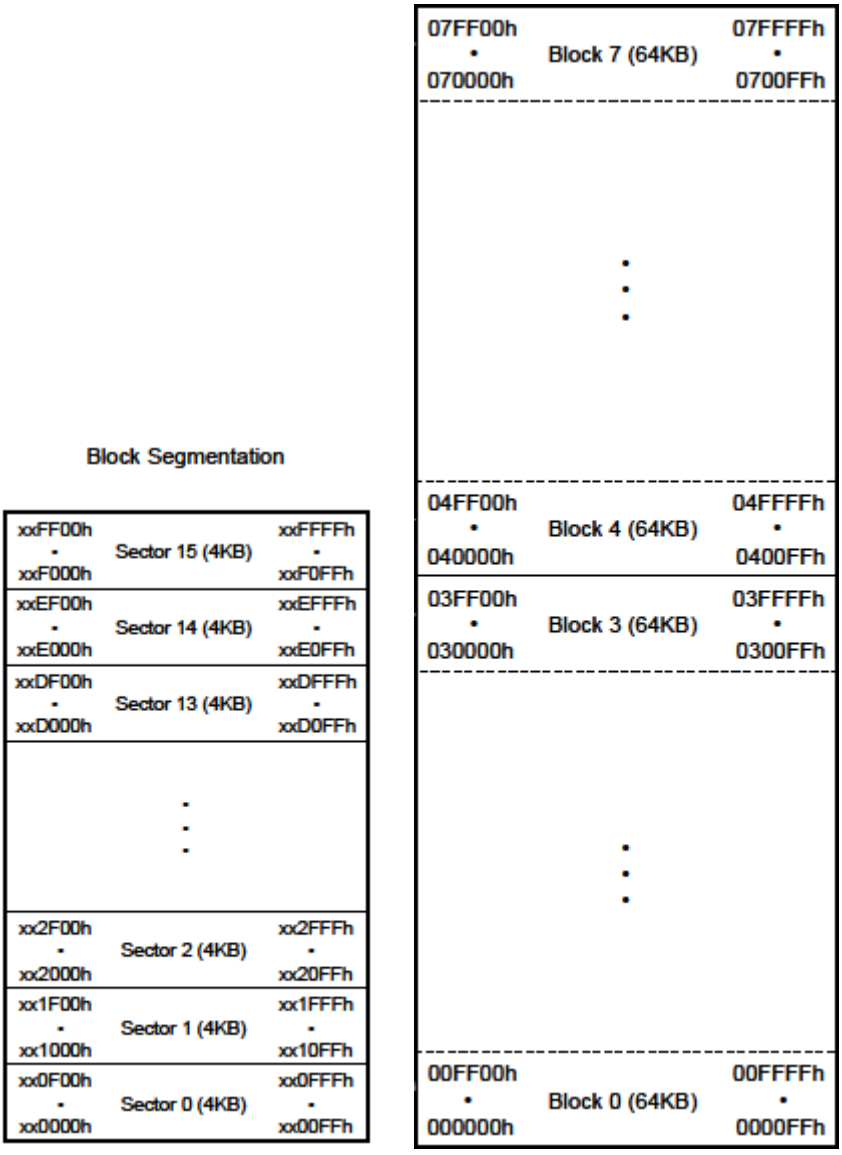
6 SERIAL FLASH MEMORY CONTROLLER

6.1 Serial Flash Memory

Serial Flash memory supports Eon and Winbond products which are driven by Quad SPI. The memory capacity limit is 16MBytes, and the memory operation speed is up to 80Mhz. However, since the Flash Memory Controller uses the AHB clock in a divided manner, it operates by 2 times the maximum system clock.

SEM8310S has 512KBytes of Serial Flash Memory. Each sector consists of 128 sectors of 4Kbytes.

6.2 Memory Architecture



6.3 Register Description

Serial Flash Mode Register (SFMOD)

Address : 0x8000_0000

Bit	R/W	Description	Default Value
31:9	R	Reserved	-
8	R/W	Chip select control 1: Chip select signal is controlled by H / W 0: Chip select is fixed as Low level	1b
7	R/W	Bus Error Enable 1: Bus error occurs when write access to serial flash occurs 0: Allow writing to Serial Flash	1b
6	R	Reserved	-
5	R	EQIO Mode Flag 1: EQIO Mode 0: Normal Mode When EQIO (38h) is written to the Command Register, Serial Flash switches to EQIO mode.	
4	R	Performance Enhance Mode 1: Performance Enhance Mode is applied. 0: Normal Mode. Not applicable. When Performance Enhance Mode is enabled by writing 1 to SFPEM Register, it is applied only when it is Quad Read or EQIO mode.	
3	R/W	Bus Ready Control 0: For write operation, control bus ready. S / W does not need to check flash status. 1: After writing, set to check flash status in S / W.	0b
2	R	Reserved	-
1:0	R/W	Serial Flash Read Mode 00: Single Read Mode 01: Dual Read Mode 10: Quad Read Mode 11: Reserved	00b

Serial Flash Baudrate Register (SFBRT)

Address : 0x8000_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:4	R/W	SCK High Pulse Width The time of the High section of Serial Flash Clock Pulse The unit is the system clock. 0000: 1clock 0001: 2clocks 0010: 3clocks …	111b

		1110: 15clocks 1111: 16clocks	
3:0	R/W	SCK Low Pulse Width Serial flash clock The time of low section of pulse The unit is the system clock. 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b

Serial Flash Chip Select High Pulse Width Register (SFCSH)

Address : 0x8000_0008

Bit	R/W	Description	Default Value
31:4	R	Reserved	-
3:0	R/W	Chip Select High Pulse Width (100ns required) The deselect time of the chip select signal is determined. When the chip select signal is deselected, it should be maintained for a certain time. 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	Fh

Serial Flash Performance Enhance Mode Register (SFPEM)

Address : 0x8000_000C

Bit	R/W	Description	Default Value
31:1	R	Reserved	-
0	R/W	Performance Enhance Mode 1: Enable 0: Disable	0b

Serial Flash Command Register (SFCMD)

.Address : 0x8000_0010

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Serial Flash Command It is a register used to transfer Instruction which is only 1 byte among Instruction transmitted to Serial Flash. For example, Chip Erase (C7h / 60h), Power-down (B9h), and Release Power-down (ABh)	0b

Serial Flash Status Register (SFSTS)

Address : 0x8000_0014

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7	R/W	SRP0(Status Register Protect) Protection mode is specified by combination with SRP1 bit.	0
6	R/W	SEC (Sector/Block Protect)	0
5	R/W	TB (Top/Bottom Protect)	0
4 : 2	R/W	BP (Block Protect)	000
1	R	WEL (Write Enable Latch) It is a bit that allows program or erase operation of flash memory. 1 : write enable 0 : write disable	0
0	R	BUSY (Erase/Write In Progress) It is a bit to check whether program or erase operation of flash memory is completed. 1 : Write operation 0 : Not in write operation	0

This register accesses the status register of Winbond flash memory which is MCP a nd is used to write or read the value. The SEC, TB, and BP bits are bits set to specif y the write protection area for the flash memory.

STATUS REGISTER(1)					W25Q40BV (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000h – 07FFFFh	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000h – 07FFFFh	128KB	Upper 1/4
0	0	0	1	1	4 thru 7	040000h – 07FFFFh	256KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/8
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/4
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/2
0	X	1	X	X	0 thru 7	000000h – 07FFFFh	512KB	ALL
1	0	0	0	1	7	07F000h – 07FFFFh	4KB	Top Block
1	0	0	1	0	7	07E000h – 07FFFFh	8KB	Top Block
1	0	0	1	1	7	07C000h – 07FFFFh	16KB	Top Block
1	0	1	0	X	7	078000h – 07FFFFh	32KB	Top Block
1	0	1	1	0	7	078000h – 07FFFFh	32KB	Top Block
1	1	0	0	1	0	000000h – 000FFFh	4KB	Bottom Block
1	1	0	1	0	0	000000h – 001FFFh	8KB	Bottom Block
1	1	0	1	1	0	000000h – 003FFFh	16KB	Bottom Block
1	1	1	0	X	0	000000h – 007FFFh	32KB	Bottom Block
1	1	1	1	0	0	000000h – 007FFFh	32KB	Bottom Block
1	X	1	1	1	0 thru 7	000000h – 07FFFFh	512KB	ALL

Serial Flash Sector Erase Address Register (SFSEA)

Address : 0x8000_0018

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Serial Flash Sector Address to Erase It is used to erase serial flash in sector unit. When the address of the sector to erase in this register is written, the selected sector is erased. At this time, Sector Erase Command is automatically generated by Serial Flash Controller.	0b

Serial Flash Block Erase Address Register (SFBEA)

Address : 0x8000_001C

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Serial Flash Block Address to Erase It is used to erase serial flash in block unit. When the address of the block to erase in this register is written, the selected block is erased. At this time, the Block Erase Command is automatically generated by the Serial Flash Controller	0b

Serial Flash Data Register (SFDAT)

Address : 0x8000_0020

Bit	R/W	Description	Default Value
31:0	R/W	Serial Flash Data This register is useful when sending instructions combined with n bytes or when receiving n byte combined responses. Note that SFMOD [8] must be set to 0 because the #CS pin of Serial Flash must be held low during the time that the instruction is sent and the response is received.	

Serial Flash WIP Check Period Register (SFWCP)

Address : 0x8000_0024

Bit	R/W	Description	Default Value
31:0	R/W	Serial Flash WIP Status Check Period	FFFh

		This is a register that sets the check period when the Serial Flash Controller automatically checks whether the corresponding operation is completed when an operation to program or erase Serial Flash Memory is performed.	

Serial Flash Clock Delay Register (SFCKDLY)

Address : 0x8000_0028

Bit	R/W	Description	Default Value
3:0	R/W	Serial Flash Feed-back Clock Delay Value It is a register that applies a delay component to the sampling clock by a user-specified amount to correct sampling timing of serial flash input data. 0 : 0 step delay 1 : 1 step delay … 15 : 15 step delay	0h

Serial Flash 2nd Status Register (SFSTS2)

Address : 0x8000_002C

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7	R	SUS(Suspend Status) Suspend Indicates the status of Erase / Program Suspend by Instruction. 0 : Not Suspend 1 : Erase/Program Suspend	0
6	R/W	CMP (Complement Protect) SEC, TB, BP2, and BP1. 0 : No effect 1 : Revese	0
5 : 2	R	LB (Security register Lock bit) The 4 bits of LB are used to write protect each of 4 security registers. Once set, they can not be reset to 0.	0
1	R/W	QE (Quad Enable) This is a bit that allows Quad operation of Flash Memory. 1 : Quad Enable 0 : Quad Disable	0
0	R/W	SRP1 (Status register protect) Protection mode is designated by combination with bit SRP0.	0

Serial Flash JEDEC ID Read Register (SFIDR)

Address : 0x8000_0040

Bit	R/W	Description	Default Value
23:0	R	Serial Flash JEDEC ID This register is used to check the JEDEC ID of Serial Flash. It consists of 3bytes. When read, it means Manufacturer, Memory type, Capacity from lower 1 byte.	0h

7 COPROCESSOR

The coprocessor includes a memory management unit (MMU) for memory management, an I-Cache, and a D-Cache functional block, and is responsible for controlling these functional blocks and other additional functional blocks.

Key Features

- Memory Management Unit
  - Real Memory mode
- Direct Cache
  - 4KBytes I-Cache
  - Write Back / Write Through
  - 16 Bytes / Line
  - LRU Replacement
  - Cache Invalidation by Software
- 4 Words Deep Write Buffer (FIFO)

Real Memory mode allows only the CPU to access some memory areas reserved for a linear memory area of 4GB size, and the address of the CPU coincides with the actual memory address.

Table 6.3-1 Real Memory map

Address Range (512KBytes)	*Sector Number*	*Size*
0x0000_0000~0x0007_FFFF (Memory Bank0)	Serial Flash	512KBytes
0x2000_0000~0x3FFF_FFFF (Memory Bank1)	Internal SRAM	16KBytes
0x4000_0000~0xFFFF_FFFF	Reserved	-

7.1 Coprocessor Description

Table 7.1-1 Coprocessor Register Description

Register	R/W	Description
SCPR15	R	System Coprocessor Status Register
	W	Master Command Register
SCPR14	R/W	Supervisor Stack Point Register
SCPR13	R/W	User Stack Pointer
SCPR12	R/W	Vector Base Register
SCPR11	W	Invalidate Cache Line and Lock Register
SCPR10	-	Reserved
SCPR9	R/W	Memory Bank Configuration Register
SCPR8	R/W	Sub-Bank Configuration Register
SCPR7	R/W	Reserved
SCPR6	R/W	Reserved
SCPR5	R/W	Sub-Bank Address Register
SCPR4	R/W	General Access Point Data Register
SCPR3	R/W	General Access Point Index Register
SCPR2	R/W	Reserved
SCPR1	R/W	Reserved
SCPR0	R/W	Reserved

7.2 Coprocessor Control Registers

System Coprocessor Status Register (SCPR15)

Bit	R/W	Description	Default Value
31	R	System Co-Processor Access Right (Privileged) Coprocessor indicates access authority. 0 : Supervisor/User Accessable 1 : Supervisor Access only	1
30 : 28	R	Coprocessor Type	001
27 : 25	R	Coprocessor Subtype	000
24 : 19	R	Reserved	-
18	R	L1 Cache Presented 0 : Presented 1 : Not Presented	0
17	R	L1 Cache Snooping Capability 0 : Support Snooping 1 : Not support Snooping	1
16	R	L1 Cache Replacement Policy 0 : Support Write-through only 1 : Support Write-through and Write-back	1
15 : 7	R	Reserved	-
6	R	Misalign Correction Support for Data Access 0 : Not support Misalign Correction 1 : Support Misalign Correction	0
5 : 2	R	SCP Rending Exception Number 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access – Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : N/A	1111
1	R	SCP Pending Exception status 0 : No Pending Exception 1 : Pending Exception Exist	0
0	R	Reserved	-

Master Command Register (SCPR15)

Bit	R/W	Description	Default Value
31 : 6	W	Reserved	-
5 : 2	W	End of Exception 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access – Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : Privilege Violation Exception	1111
1 : 0	W	Reserved	-

Supervisor Stack Point Register (SCPR14)

Bit	R/W	Description	Default Value
31 : 2	R/W	Supervisor Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

User Stack Point Register (SCPR13)

Bit	R/W	Description	Default Value
31 : 2	R/W	User Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

Vector Base Register (SCPR12)

Bit	R/W	Description	Default Value
31 : 2	R/W	Vector Base for Exception	0x0000_0000
1 : 0	R/W	Always 0	00

Invalidate Cache Line and Lock Register (SCPR11)

Bit	R/W	Description	Default Value
31 : 7	W	Invalidation Target Address/Way	-
6 : 4	W	Invalidation Target Address/Way	-
3	W	Invalidation Mode 0 : Address Based Invalidation 1 : Way Based Invalidation	-
2	W	Copy-back Selection in Invalidation 0 : Invalidation without Copy-back 1 : Invalidation with Copy-back if need	-
1	W	Cache Line Locking in Invalidation 0 : Invalidation without Locking 1 : Invalidation with Locking	-
0	W	Cache Type in Invalidation 0 : I-Cache 1 : D-Cache	-

Memory Bank Configuration Register (SCPR9)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	0
15	R/W	Always 0	0
14	R/W	Memory Bank 3 Access Right 0 : Supervisor only Accessable 1 : Supervisor/User Accessable	0
13 : 12	R/W	Memory Bank 3 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : Enable Cache with Write-back	00
11	R/W	Always 0	0
10	R/W	Memory Bank 2 Access Right 0 : Supervisor only Accessable 1 : Supervisor/User Accessable	0
9 : 8	R/W	Memory Bank 2 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : Enable Cache with Write-back	00
7	R/W	Always 0	0
6	R/W	Memory Bank 1 Access Right 0 : Supervisor only Accessable 1 : Supervisor/User Accessable	0
5 : 4	R/W	Memory Bank 1 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : Enable Cache with Write-back	00
3	R/W	Always 0	0
2	R/W	Memory Bank 0 Access Right 0 : Supervisor only Accessable 1 : Supervisor/User Accessable	0
1 : 0	R/W	Memory Bank 0 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : Enable Cache with Write-back	00

Sub-Bank Configuration Register (SCPR8)

Bit	R/W	Description	Default Value
31 : 7	R	Reserved	-
6 : 4	R/W	Sub-Bank Index	000
3	R/W	Sub-Bank Valid Control bit 0 : Invalid 1 : Valid	0
2	R/W	Sub-Bank Access Right 0 : Supervisor only Accessable 1 : Supervisor/User Accessable	0
1 : 0	R/W	Sub-Bank Cache Property Control bit 00 : Disable Cache, Disable Write buffer 01 : Disable Cache, Enable Write buffer 10 : Enable Cache with Write-through 11 : Enable Cache with Write-back	00

*** It is set with SCPR5 to designate sub-bank.
*** In the area where the sub-bank is set, the sub-bank setting information has priority over the setting of the memory bank set in SCPR9.

Sub-Bank Address Register (SCPR5)

Bit	R/W	Description	Default Value
31 : 12	R/W	Sub-Bank Base Address[31:12]	0x00000
11 : 0	R/W	Sub-Bank Size Enable 0x000 : 4KBytes 0x001 : 8KBytes 0x003 : 16KBytes 0x007 : 32KBytes 0x00F : 64KBytes 0x01F : 128KBytes 0x03F : 256KBytes 0x07F : 512KBytes 0x0FF : 1MBytes	0x000

*** Must be set to Nature Align when setting Sub-Bank.

General Access Point Data Register (SCPR4)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Data The value of register set in SCPR3	0x0000_0000

General Access Point Index Register (SCPR3)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Index - Core Debugging Information 0x0000_0000 : Backup IR 0x0000_0001 : Backup ER 0x0000_0002 : Backup PC 0x0000_0010 : Backup EAD - System Coprocessor Debugging Information 0x0000_0303 : Inst. Bus Error Address 0x0000_0304 : Data Bus Error Address - Cache Lock Information 0x0000_0500 : Inst. Lock Condition 0x0000_0501 : Data Lock Condition - Memory Bank Management Information 0x0000_0600 : Inst. MBMB Violation Address 0x0000_0601 : Data MBMB Violation Address - SPM Management Information 0x0000_0700~0x0000_0736: See Register below	-

**********SPM Management Register**********

Global SPM Control Register(GSPMSCR)

Address : 0x0000_0700

Bit	R/W	Description	Default Value
31 : 28	R	Exception Status 4'b0001 : DATA Access Violation 4'b0010 : Instruction Access Violation	0h
27 : 24	R	Reserved	0h
23 : 20	R/W	iBank Size: Physical memory size of each bank in iSPM 4'h0: 1KB 4'h1: 2KB 4'h2: 4KB 4'h3: 8KB 4'h4: 16KB 4'h5: 32KB	

		4'h6: 64KB 4'h7: 128KB 4'h8: 256KB	
19 : 16	R/W	iSPM Configuration 4'h0: Appears as one chunk of memory to the user 4'h1: Reserved 4'h2: Appears to the user as four chunks of memory	0h
15 : 12	R/W	iSPM Enable 4'h1 : SPM Enable 4'h0 : SPM Disable	0h
11 : 8	R/W	iBank Size: Physical memory size of each bank in iSPM 4'h0: 1KB 4'h1: 2KB 4'h2: 4KB 4'h3: 8KB 4'h4: 16KB 4'h5: 32KB 4'h6: 64KB 4'h7: 128KB 4'h8: 256KB	
7 : 4	R/W	iSPM Configuration 4'h0: Appears as one chunk of memory to the user 4'h1: Reserved 4'h2: Appears to the user as four chunks of memory	
3 : 0	R/W	iSPM Enable 4'h1 : SPM Enable 4'h0 : SPM Disable	

Local SPM Control Register(LSPMSCR)

Address : 0x0000_0701, 0x0000_0711,0x0000_0721, 0x000_0731 – iSPM

Address : 0x0000_0704, 0x0000_0714,0x0000_0724 ,0x000_0734 – dSPM

Bit	*R/W*	*Description*	*Default Value*
31 : 12	R	Reserved	0h
11 : 8	R	External Access: BUS access 4'h0 : External Access Not Support 4'h1 : External Access Support	
7 : 4	R/W	Privilege Mode: User rights 4'h0 : Supervisor Only Access 4'h1 : Supervisor/User Access	0h
3 : 0	R/W	Enable 4'h1 : Local SPM Enable	0h

		4'h0 : Local SPM Disable	

Local SPM Start Register (LSPMSR)

Address : 0x0000_0702, 0x0000_0712,0x0000_0722, 0x000_0732 – iSPM

Address : 0x0000_0705, 0x0000_0715,0x0000_0725 ,0x000_0735 – dSPM

Bit	R/W	Description	Default Value
31 : 0	R/W	SPM Start Address	0h

Local SPM End Register (LSPMER)

Address : 0x0000_0703, 0x0000_0713,0x0000_0723, 0x000_0733 –iSPM

Address : 0x0000_0706, 0x0000_0716,0x0000_0726, 0x000_0736 – dSPM

Bit	R/W	Description	Default Value
31 : 0	R/W	SPM End Address	0h

*** For End Address Register, be sure to set the Start Address Register first.

8 INTERRUPTS

It has 24 channels of interrupt inputs, consisting of 21 interrupts and 3 external interrupts from internal devices such as Timer, SPI, TWI, UART, etc.

Key Features

- 24 channels of interrupts (3 channels of external interrupts and 21 channels of internal interrupts)
- Operation condition setting for external interrupt (5 kinds)
- Operation condition setting for internal interrupt (2 kinds)
- Interrupt enable function for each channel
- Interrupt Mask function for each channel
- Individually programmable interrupt priority

The sequential processing of interrupts is done through the following process.

1. Each interrupt source requests an interrupt to the interrupt controller.
2. It is selected by Interrupt Enable Register, and then it is stored in Interrupt Pending Register.
3. After determining the interrupt priority, request an interrupt to the CPU.
4. When an interrupt is requested, the CPU's interrupt is disabled and reads the interrupt vector address and enters the corresponding Interrupt Service Routine (ISR).
5. Perform ISR.
6. When the ISR is finished, write the corresponding Vector value to the Interrupt Pending Clear Register to clear the interrupt value stored in the Interrupt Pending Register.
7. Interrupts of the CPU are activated while exiting the ISR.

Interrupt processing is performed through the following process.

1. Each interrupt source requests an interrupt to the interrupt controller.
2. It is selected by Interrupt Enable Register, and then it is stored in Interrupt Pending Register.
3. After determining the interrupt priority, request an interrupt to the CPU.
4. When an interrupt is requested, the CPU's interrupt is disabled and reads the interrupt vector address and enters the corresponding Interrupt Service Routine (ISR).
5. To allow overlapping of interrupts, clear the interrupt value stored in the Interrupt Pending Register by writing the corresponding Vector value to the Interrupt Pending Clear Register and activate the CPU's interrupt via asm ("set 13").
6. Perform ISR.
7. If interrupts occur again during the execution of the current ISR, overlap processing is allowed and the corresponding ISR is entered.
8. When execution of the newly entered ISR finishes, it returns to the previous ISR and proceeds with the remaining execution.
9. When the ISR is done, it exits completely

8.1 Interrupt Vector and Priority

Interrupt priority is highest in EIRQ0. The interrupt vector address has a size of 4 bytes each because the CPU performs 32-bit addressing.

Table 8.1-1 Interrupt Vector & Priority

Vector No.	Description	Vector Address
0x3F	Reserved	0x000000FC
0x3E	Reserved	0x000000F8
0x3D	UART2 Interrupt	0x000000F4
0x3C	Reserved	0x000000F0
0x3B	Watch-Dog Timer Interrupt	0x000000EC
0x3A	KeyScan Interrupt	0x000000E8
0x39	GPIO2 Interrupt	0x000000E4
0x38	Reserved	0x000000E0
0x37	TIMER2 Interrupt	0x000000DC
0x36	PMU Interrupt	0x000000D8
0x35	Temp Interrupt	0x000000D4
0x34	Reserved	0x000000D0
0x33	RTC Interrupt	0x000000CC
0x32	Filter Interrupt	0x000000C8
0x31	UART1 Interrupt	0x000000C4
0x30	Reserved	0x000000C0
0x2F	GPIO1 Interrupt	0x000000BC
0x2E	TIMER1 Interrupt	0x000000B8
0x2D	TWI Interrupt	0x000000B4
0x2C	Reserved	0x000000B0
0x2B	SPI Interrupt	0x000000AC
0x2A	SAG Interrupt	0x000000A8
0x29	PFAIL Interrupt	0x000000A4
0x28	EIRQ2 Interrupt	0x000000A0
0x27	UART0 Interrupt	0x0000009C
0x26	GPIO0 Interrupt	0x00000098
0x25	TIMER0 Interrupt	0x00000094
0x24	EIRQ1 Interrupt	0x00000090
0x23	ADC Interrupt	0x0000008C
0x22	EMB Interrupt	0x00000088
0x21	Reserved	0x00000084
0x20	EIRQ0 Interrupt (Highest Priority)	0x00000080

8.2 External Interrupt

External Interrupt accepts five types of external interrupts by setting the EINTMOD register.

- In low level mode, interrupt occurs every system cycle while External Interrupt signal is kept "Low".
- In High Level Mode, an interrupt is generated every system cycle while the External Interrupt signal remains "High".
- In Falling Edge Mode, an interrupt is generated when the External Interrupt signal changes from "High-> Low".
- In Rising Edge Mode, an interrupt occurs when the External Interrupt signal changes from "Low-> High".
- In Any Edge mode, an interrupt is generated when the external interrupt signal changes from "High-> Low" or "Low-> High".

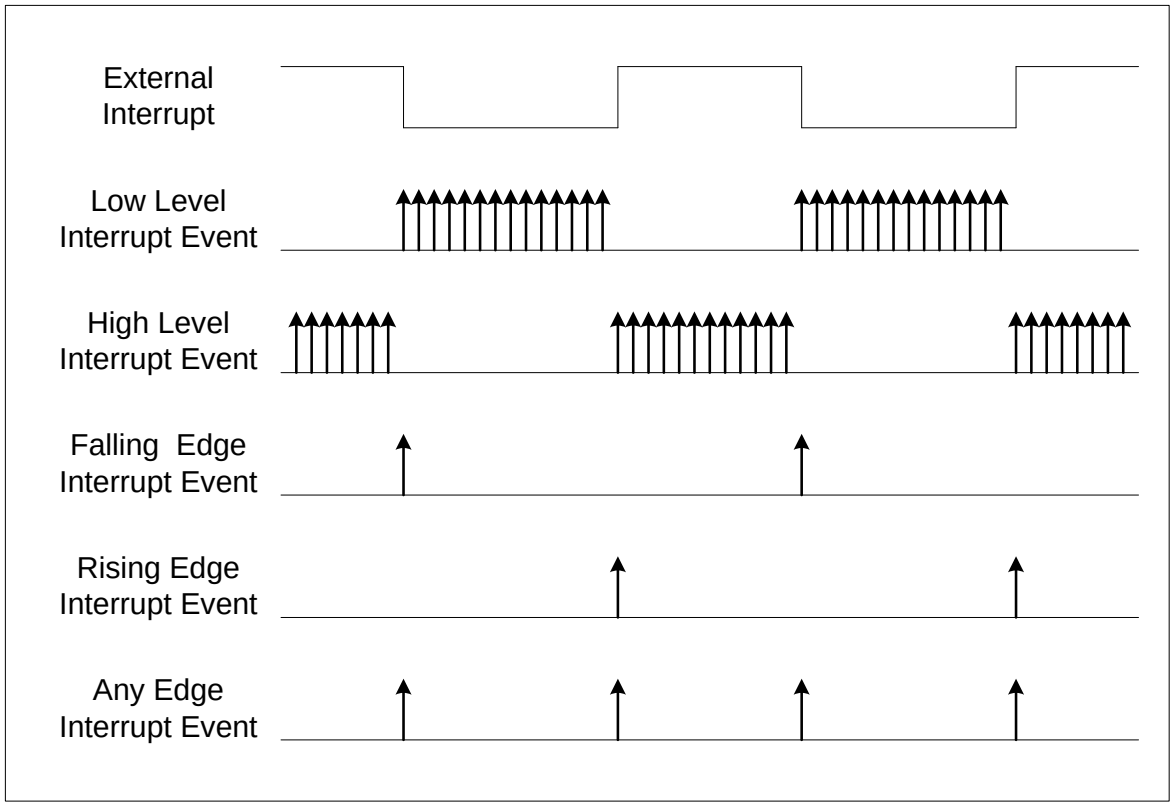


Figure 8-1 External Interrupt Mode

8.3 Internal Interrupt Mode

All internal interrupts operate as "Rising Edge". However, if the user wants to process the interrupt with "High Level", it can be set through the Internal Interrupt Mode Registers.

8.4 Interrupt Pending and Interrupt Pending Clear

The occurrence status of each interrupt can be confirmed by Interrupt Pending Registers. Interrupts that occur once are stored in the Interrupt Pending Register until they are cleared by the Interrupt Pending Clear Register. Also, if an interrupt with a higher priority than the currently generated interrupt is stored in the interrupt pending registers without being masked, it is stored in Interrupt Pending Registers until all the high priority interrupts are cleared.

To clear the interrupts stored in the Interrupt Pending Registers, write the corresponding interrupt vector number value through the Interrupt Pending Clear Register.

8.5 Interrupt Enable

Interrupts masked by the Interrupt Mask Registers are still stored in the Interrupt Pending Registers, while interrupts disabled by the Interrupt Enable Registers (IENR) are not stored in the Interrupt Pending Registers. Therefore, this register is used to disable interrupts that you do not want to accept at all.

8.6 Interrupt Mask Set/Clear Register

If set, request is enabled. If clear, request is disabled.

Each interrupt can perform a request for the corresponding interrupt by the Interrupt Mask Registers. When the Interrupt Mask Set bit is "1", the CPU requests the interrupt stored in the Interrupt Pending Register. When the Interrupt Mask Clear bit is "1", it can not request the interrupt stored in the Interrupt Pending Register to the CPU.

Even if an interrupt whose mask bit is set to "0" is stored in the Interrupt Pending Registers (IPR), if the mask bit is reset to "1", the interrupt stored in the Interrupt Pending Registers requests the interrupt again by priority.

8.7 Interrupt Control Registers

Interrupt Pending Clear Register (PENDCLR)

Address : 0xFFFF_0000

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	W	Interrupt Pending Register Clear Value (0x20 ~ 0x3F)	0xFF

*** To clear the Interrupt Pending Register, It should be clear by value. (See Interrupt Vector No.)

External Interrupt Mode and External PIN Level Register (EINTMOD)

Address : 0xFFFF_0004

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23	R	EIRQ5ST : EIRQ5 PIN Level	-
22 : 20	R/W	EIRQ5MOD : EIRQ5 Active State	010
19	R	EIRQ4ST : EIRQ4 PIN Level	-
18 : 16	R/W	EIRQ4MOD : EIRQ4 Active State	010
15	R	EIRQ3ST : EIRQ3 PIN Level	-
14 : 12	R/W	EIRQ3MOD : EIRQ3 Active State	010
11	R	EIRQ2ST : EIRQ2 PIN Level	-
10 : 8	R/W	EIRQ2MOD : EIRQ2 Active State	010
7	R	EIRQ1ST : EIRQ1 PIN Level	-
6 : 4	R/W	EIRQ1MOD : EIRQ1 Active State	010
3	R	EIRQ0ST : EIRQ0 PIN Level	-
2 : 0	R/W	EIRQ0MOD : EIRQ0 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010

Internal Interrupt Mode Register (IINTMOD)

Address : 0xFFFF_0008

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F Interrupt Mode bit	0
30	R/W	Vector No. 0x3E Interrupt Mode bit	0
29	R/W	Vector No. 0x3D Interrupt Mode bit	0
28	-	Reserved	-
27	R/W	Vector No. 0x3B Interrupt Mode bit	0
26	R/W	Vector No. 0x3A Interrupt Mode bit	0
25	R/W	Vector No. 0x39 Interrupt Mode bit	0
24	-	Reserved	-
23	R/W	Vector No. 0x37 Interrupt Mode bit	0
22	R/W	Vector No. 0x36 Interrupt Mode bit	0
21	R/W	Vector No. 0x35 Interrupt Mode bit	0
20	-	Reserved	-
19	R/W	Vector No. 0x33 Interrupt Mode bit	0
18	R/W	Vector No. 0x32 Interrupt Mode bit	0
17	R/W	Vector No. 0x31 Interrupt Mode bit	0
16	-	Reserved	-
15	R/W	Vector No. 0x2F Interrupt Mode bit	0
14	R/W	Vector No. 0x2E Interrupt Mode bit	0
13	R/W	Vector No. 0x2D Interrupt Mode bit	0
12	-	Reserved	-
11	R/W	Vector No. 0x2B Interrupt Mode bit	0
10	R/W	Vector No. 0x2A Interrupt Mode bit	0
9	R/W	Vector No. 0x29 Interrupt Mode bit	0
8	-	Reserved	-
7	R/W	Vector No. 0x27 Interrupt Mode bit	0
6	R/W	Vector No. 0x26 Interrupt Mode bit	0
5	R/W	Vector No. 0x25 Interrupt Mode bit	0
4	-	Reserved	-
3	R/W	Vector No. 0x23 Interrupt Mode bit	0
2	R/W	Vector No. 0x22 Interrupt Mode bit	0
1	R/W	Vector No. 0x21 Interrupt Mode bit	0
0	-	Reserved	-

*** Internal Interrupt Mode bit

0 : High Level Mode

1 : Rising Edge Mode

Interrupt Pending Register (INTPEND)

Address : 0xFFFF_000C

Bit	R/W	Description	Default Value
31	R	Vector No. 0x3F Interrupt Pending bit	-
30	R	Vector No. 0x3E Interrupt Pending bit	-
29	R	Vector No. 0x3D Interrupt Pending bit	-
28	R	Vector No. 0x3C Interrupt Pending bit	-
27	R	Vector No. 0x3B Interrupt Pending bit	-
26	R	Vector No. 0x3A Interrupt Pending bit	-
25	R	Vector No. 0x39 Interrupt Pending bit	-
24	R	Vector No. 0x38 Interrupt Pending bit	-
23	R	Vector No. 0x37 Interrupt Pending bit	-
22	R	Vector No. 0x36 Interrupt Pending bit	-
21	R	Vector No. 0x35 Interrupt Pending bit	-
20	R	Vector No. 0x34 Interrupt Pending bit	-
19	R	Vector No. 0x33 Interrupt Pending bit	-
18	R	Vector No. 0x32 Interrupt Pending bit	-
17	R	Vector No. 0x31 Interrupt Pending bit	-
16	R	Vector No. 0x30 Interrupt Pending bit	-
15	R	Vector No. 0x2F Interrupt Pending bit	-
14	R	Vector No. 0x2E Interrupt Pending bit	-
13	R	Vector No. 0x2D Interrupt Pending bit	-
12	R	Vector No. 0x2C Interrupt Pending bit	-
11	R	Vector No. 0x2B Interrupt Pending bit	-
10	R	Vector No. 0x2A Interrupt Pending bit	-
9	R	Vector No. 0x29 Interrupt Pending bit	-
8	R	Vector No. 0x28 Interrupt Pending bit	-
7	R	Vector No. 0x27 Interrupt Pending bit	-
6	R	Vector No. 0x26 Interrupt Pending bit	-
5	R	Vector No. 0x25 Interrupt Pending bit	-
4	R	Vector No. 0x24 Interrupt Pending bit	-
3	R	Vector No. 0x23 Interrupt Pending bit	-
2	R	Vector No. 0x22 Interrupt Pending bit	-
1	R	Vector No. 0x21 Interrupt Pending bit	-
0	R	Vector No. 0x20 Interrupt Pending bit	-

*** The value of each bit in the Interrupt Pending Register indicates that the corresponding interrupt has occurred. The value of the Interrupt Pending Register is cleared by the Interrupt Pending Clear register. Normally it is cleared at the end of the corresponding interrupt.

Interrupt Enable Register (INTEN)

Address : 0xFFFF_0010

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F Interrupt Enable bit	0
30	R/W	Vector No. 0x3E Interrupt Enable bit	0
29	R/W	Vector No. 0x3D Interrupt Enable bit	0
28	R/W	Vector No. 0x3C Interrupt Enable bit	0
27	R/W	Vector No. 0x3B Interrupt Enable bit	0
26	R/W	Vector No. 0x3A Interrupt Enable bit	0
25	R/W	Vector No. 0x39 Interrupt Enable bit	0
24	R/W	Vector No. 0x38 Interrupt Enable bit	0
23	R/W	Vector No. 0x37 Interrupt Enable bit	0
22	R/W	Vector No. 0x36 Interrupt Enable bit	0
21	R/W	Vector No. 0x35 Interrupt Enable bit	0
20	R/W	Vector No. 0x34 Interrupt Enable bit	0
19	R/W	Vector No. 0x33 Interrupt Enable bit	0
18	R/W	Vector No. 0x32 Interrupt Enable bit	0
17	R/W	Vector No. 0x31 Interrupt Enable bit	0
16	R/W	Vector No. 0x30 Interrupt Enable bit	0
15	R/W	Vector No. 0x2F Interrupt Enable bit	0
14	R/W	Vector No. 0x2E Interrupt Enable bit	0
13	R/W	Vector No. 0x2D Interrupt Enable bit	0
12	R/W	Vector No. 0x2C Interrupt Enable bit	0
11	R/W	Vector No. 0x2B Interrupt Enable bit	0
10	R/W	Vector No. 0x2A Interrupt Enable bit	0
9	R/W	Vector No. 0x29 Interrupt Enable bit	0
8	R/W	Vector No. 0x28 Interrupt Enable bit	0
7	R/W	Vector No. 0x27 Interrupt Enable bit	0
6	R/W	Vector No. 0x26 Interrupt Enable bit	0
5	R/W	Vector No. 0x25 Interrupt Enable bit	0
4	R/W	Vector No. 0x24 Interrupt Enable bit	0
3	R/W	Vector No. 0x23 Interrupt Enable bit	0
2	R/W	Vector No. 0x22 Interrupt Enable bit	0
1	R/W	Vector No. 0x21 Interrupt Enable bit	0
0	R/W	Vector No. 0x20 Interrupt Enable bit	0

*** Interrupt Enable bit

0 : Interrupt Disable

1 : Interrupt Enable

Interrupt Mask Status Register (INTMASK)

Address : 0xFFFF_0014

Bit	R/W	Description	Default Value
31 : 0	R	Interrupt Mask Status Register	0x0000_0000

*** You can check the status of all mask bits.

Interrupt Mask Set Register (MASKSET)

Address : 0xFFFF_0014h

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F Interrupt Request Set bit	0
30	W	Vector No. 0x3E Interrupt Request Set bit	0
29	W	Vector No. 0x3D Interrupt Request Set bit	0
28	W	Vector No. 0x3C Interrupt Request Set bit	0
27	W	Vector No. 0x3B Interrupt Request Set bit	0
26	W	Vector No. 0x3A Interrupt Request Set bit	0
25	W	Vector No. 0x39 Interrupt Request Set bit	0
24	W	Vector No. 0x38 Interrupt Request Set bit	0
23	W	Vector No. 0x37 Interrupt Request Set bit	0
22	W	Vector No. 0x36 Interrupt Request Set bit	0
21	W	Vector No. 0x35 Interrupt Request Set bit	0
20	W	Vector No. 0x34 Interrupt Request Set bit	0
19	W	Vector No. 0x33 Interrupt Request Set bit	0
18	W	Vector No. 0x32 Interrupt Request Set bit	0
17	W	Vector No. 0x31 Interrupt Request Set bit	0
16	W	Vector No. 0x30 Interrupt Request Set bit	0
15	W	Vector No. 0x2F Interrupt Request Set bit	0
14	W	Vector No. 0x2E Interrupt Request Set bit	0
13	W	Vector No. 0x2D Interrupt Request Set bit	0
12	W	Vector No. 0x2C Interrupt Request Set bit	0
11	W	Vector No. 0x2B Interrupt Request Set bit	0
10	W	Vector No. 0x2A Interrupt Request Set bit	0
9	W	Vector No. 0x29 Interrupt Request Set bit	0
8	W	Vector No. 0x28 Interrupt Request Set bit	0
7	W	Vector No. 0x27 Interrupt Request Set bit	0
6	W	Vector No. 0x26 Interrupt Request Set bit	0
5	W	Vector No. 0x25 Interrupt Request Set bit	0
4	W	Vector No. 0x24 Interrupt Request Set bit	0
3	W	Vector No. 0x23 Interrupt Request Set bit	0
2	W	Vector No. 0x22 Interrupt Request Set bit	0
1	W	Vector No. 0x21 Interrupt Request Set bit	0
0	W	Vector No. 0x20 Interrupt Request Set bit	0

*** Interrupt Request Set bit

0 : No Effect interrupt Mask.

1 : Pending interrupt is allowed to become active (interrupts sent to CPU).

Interrupt Mask Clear Register (MASKCLR)

Address : 0xFFFF_0018

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F Interrupt Request Clear bit	0
30	W	Vector No. 0x3E Interrupt Request Clear bit	0
29	W	Vector No. 0x3D Interrupt Request Clear bit	0
28	W	Vector No. 0x3C Interrupt Request Clear bit	0
27	W	Vector No. 0x3B Interrupt Request Clear bit	0
26	W	Vector No. 0x3A Interrupt Request Clear bit	0
25	W	Vector No. 0x39 Interrupt Request Clear bit	0
24	W	Vector No. 0x38 Interrupt Request Clear bit	0
23	W	Vector No. 0x37 Interrupt Request Clear bit	0
22	W	Vector No. 0x36 Interrupt Request Clear bit	0
21	W	Vector No. 0x35 Interrupt Request Clear bit	0
20	W	Vector No. 0x34 Interrupt Request Clear bit	0
19	W	Vector No. 0x33 Interrupt Request Clear bit	0
18	W	Vector No. 0x32 Interrupt Request Clear bit	0
17	W	Vector No. 0x31 Interrupt Request Clear bit	0
16	W	Vector No. 0x30 Interrupt Request Clear bit	0
15	W	Vector No. 0x2f Interrupt Request Clear bit	0
14	W	Vector No. 0x2E Interrupt Request Clear bit	0
13	W	Vector No. 0x2D Interrupt Request Clear bit	0
12	W	Vector No. 0x2C Interrupt Request Clear bit	0
11	W	Vector No. 0x2B Interrupt Request Clear bit	0
10	W	Vector No. 0x2A Interrupt Request Clear bit	0
9	W	Vector No. 0x29 Interrupt Request Clear bit	0
8	W	Vector No. 0x28 Interrupt Request Clear bit	0
7	W	Vector No. 0x27 Interrupt Request Clear bit	0
6	W	Vector No. 0x26 Interrupt Request Clear bit	0
5	W	Vector No. 0x25 Interrupt Request Clear bit	0
4	W	Vector No. 0x24 Interrupt Request Clear bit	0
3	W	Vector No. 0x23 Interrupt Request Clear bit	0
2	W	Vector No. 0x22 Interrupt Request Clear bit	0
1	W	Vector No. 0x21 Interrupt Request Clear bit	0
0	W	Vector No. 0x20 Interrupt Request Clear bit	0

*** Interrupt Request Clear bit

0 : No Effect Interrupt Mask.

1 : Pending interrupt is masked from becoming active (interrupts not sent to CPU).

Programmable Interrupt Priority Enable Register (PPENR)

Address : 0xFFFF_001C

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Programmable Priority Enable bit 0 : Programmable Priority Disable 1 : Programmable Priority Enable	0

Interrupt Priority Vector 0 Register (IPVR0)

Address : 0xFFFF_0020

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x23 Interrupt Priority	0x03
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x22 Interrupt Priority	0x02
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x21 Interrupt Priority	0x01
7 : 5	R	Reserved	-
4 : 0	RW	Vector No. 0x20 Interrupt Priority	0x00

Interrupt Priority Vector 1 Register (IPVR1)

Address : 0xFFFF_0024

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x27 Interrupt Priority	0x07
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x26 Interrupt Priority	0x06
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x25 Interrupt Priority	0x05
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x24 Interrupt Priority	0x04

Interrupt Priority Vector 2 Register (IPVR2)

Address : 0xFFFF_0028

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x2B Interrupt Priority	0x0B
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x2A Interrupt Priority	0x0A
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x29 Interrupt Priority	0x09
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x28 Interrupt Priority	0x08

Interrupt Priority Vector 3 Register (IPVR3)

Address : 0xFFFF_002C

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x2F Interrupt Priority	0x0F
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x2E Interrupt Priority	0x0E
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x2D Interrupt Priority	0x0D
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x2C Interrupt Priority	0x0C

Interrupt Priority Vector 4 Register (IPVR4)

Address : 0xFFFF_0030

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x33 Interrupt Priority	0x13
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x32 Interrupt Priority	0x12
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x31 Interrupt Priority	0x11
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x30 Interrupt Priority	0x10

Interrupt Priority Vector 5 Register (IPVR5)

Address : 0xFFFF_0034

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x37 Interrupt Priority	0x17
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x36 Interrupt Priority	0x16
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x35 Interrupt Priority	0x15
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x34 Interrupt Priority	0x14

Interrupt Priority Vector 6 Register (IPVR6)

Address : 0xFFFF_0038

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x3B Interrupt Priority	0x1B
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x3A Interrupt Priority	0x1A
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x39 Interrupt Priority	0x19
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x38 Interrupt Priority	0x18

Interrupt Priority Vector 7 Register (IPVR7)

Address : 0xFFFF_003C

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28 : 24	R/W	Vector No. 0x3F Interrupt Priority	0x1F
23 : 21	R	Reserved	-
20 : 16	R/W	Vector No. 0x3E Interrupt Priority	0x1E
15 : 13	R	Reserved	-
12 : 8	R/W	Vector No. 0x3D Interrupt Priority	0x1D
7 : 5	R	Reserved	-
4 : 0	R/W	Vector No. 0x3C Interrupt Priority	0x1C

9 GPIO (GENERAL PURPOSE I/O)

GPIO I / O provides a total of 18 I / Os in two groups of 8-bit and 2-bit groups. Each I / O can be easily configured with register settings and used for various I / O applications and system configurations.

Key Features

- P0.x has 8 I/O
- P1.x has 8 I/O
- P2.x has 2 I/O

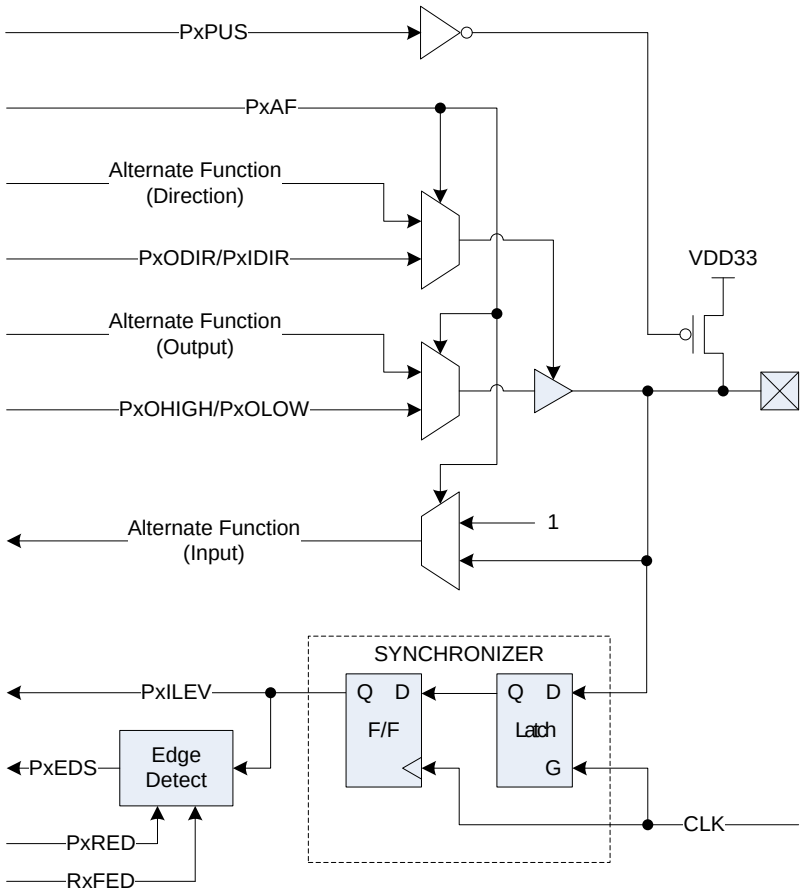


Figure 9-1 GPIO Block Diagram

9.1 In/Out Control

Output mode is set for each I / O through the PxODIR register, and input mode is set for each I / O by the PxIDIR register. The setting status of each I / O can be confirmed by the PxDIR register. When the PxODIR register and PxIDIR register are set, only the bit "1" is set as the corresponding operation, and the bit "0" has no effect.

The output level is set to Output Level through the PxOHIGH register while it is set to Output mode, and it is set to Low Level through the PxOLOW register. The setting status of the output level can be confirmed by the PxOLEV register.

The input level can be checked with the PxILEV register. The pull-up resistor connected to each I / O can reduce the leakage current when the signal level is "Low" by removing the pull-up when the external input is present or output.

Table 9.1-1 Internal Pull-up Resistance Characteristics

Parameter	*Min*	*Typ*	*Max*	*Unit*
Pull-Up Resistance	30	66	130	KΩ

9.2 Edge Detect

In addition to external interrupt via EIRQ pin, external interrupt can be performed for each group through edge detection of GPIO. Each I / O supports Rising Edge, Falling Edge, and Any Edge modes.

9.3 GPIO Registers

GPIO Direction Registers (PxDIR)

Address : 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	Px.yDIR : Px.y Direction bit 0 : Input 1 : Output	0x00

GPIO Direction Output Mode Setting Registers (PxODIR)

Address : 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7ODIR : Px.7 Direction Output Mode Setting bit	-
6	W	Px.6ODIR : Px.6 Direction Output Mode Setting bit	-
5	W	Px.5ODIR : Px.5 Direction Output Mode Setting bit	-
4	W	Px.4ODIR : Px.4 Direction Output Mode Setting bit	-
3	W	Px.3ODIR : Px.3 Direction Output Mode Setting bit	-
2	W	Px.2ODIR : Px.2 Direction Output Mode Setting bit	-
1	W	Px.1ODIR : Px.1 Direction Output Mode Setting bit	-
0	W	Px.0ODIR : Px.0 Direction Output Mode Setting bit	-

*** Direction Output Mode Setting bit

0 : No effect 1 : Set to output mode the corresponding bit in the PxDIR registers

GPIO Direction Input Mode Setting Registers (PxIDIR)

Address : 0xFFFF_3004 / 0xFFFF_3044 / 0xFFFF_3084

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7IDIR : Px.7 Direction Input Mode Setting bit	-
6	W	Px.6IDIR : Px.6 Direction Input Mode Setting bit	-
5	W	Px.5IDIR : Px.5 Direction Input Mode Setting bit	-
4	W	Px.4IDIR : Px.4 Direction Input Mode Setting bit	-
3	W	Px.3IDIR : Px.3 Direction Input Mode Setting bit	-
2	W	Px.2IDIR : Px.2 Direction Input Mode Setting bit	-
1	W	Px.1IDIR : Px.1 Direction Input Mode Setting bit	-
0	W	Px.0IDIR : Px.0 Direction Input Mode Setting bit	-

*** Direction Input Mode Setting bit

0 : No effect 1 : Set to input mode the corresponding bit in the PxDIR registers

GPIO Output Data Level Registers (PxOLEV)

Address : 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	Px.yOLEV : Px.y Output Level bit 0 : Low Level 1 : High Level	0xFF

GPIO Output Data High Level Setting Registers (PxOHIGH)

Address : 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7OH : Px.7 Output Data High Level Setting bit	-
6	W	Px.6OH : Px.6 Output Data High Level Setting bit	-
5	W	Px.5OH : Px.5 Output Data High Level Setting bit	-
4	W	Px.4OH : Px.4 Output Data High Level Setting bit	-
3	W	Px.3OH : Px.3 Output Data High Level Setting bit	-
2	W	Px.2OH : Px.2 Output Data High Level Setting bit	-
1	W	Px.1OH : Px.1 Output Data High Level Setting bit	-
0	W	Px.0OH : Px.0 Output Data High Level Setting bit	-

*** Output Data High Level Setting bit

0 : No effect

1 : Set to high level output data the corresponding bit in the PxOLEV registers

GPIO Output Data Low Level Setting Registers (PxOLOW)

Address : 0xFFFF_300C / 0xFFFF_304C / 0xFFFF_308C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7OL : Px.7 Output Data Low Level Setting bit	-
6	W	Px.6OL : Px.6 Output Data Low Level Setting bit	-
5	W	Px.5OL : Px.5 Output Data Low Level Setting bit	-
4	W	Px.4OL : Px.4 Output Data Low Level Setting bit	-
3	W	Px.3OL : Px.3 Output Data Low Level Setting bit	-
2	W	Px.2OL : Px.2 Output Data Low Level Setting bit	-
1	W	Px.1OL : Px.1 Output Data Low Level Setting bit	-
0	W	Px.0OL : Px.0 Output Data Low Level Setting bit	-

*** Output Data Low Level Setting bit

0 : No effect

1 : Set to low level output data the corresponding bit in the PxOLEV registers

GPIO Input Data Level Registers (PxILEV)

Address : 0xFFFF_3010 / 0xFFFF_3050 / 0xFFFF_3090

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	Px.7ILEV : Px.7 Input Level bit 0 : Low Level 1 : High Level	Pull-up
6	R	Px.6ILEV : Px.6 Input Level bit 0 : Low Level 1 : High Level	Pull-up
5	R	Px.5ILEV : Px.5 Input Level bit 0 : Low Level 1 : High Level	Pull-up
4	R	Px.4ILEV : Px.4 Input Level bit 0 : Low Level 1 : High Level	Pull-up
3	R	Px.3ILEV : Px.3 Input Level bit 0 : Low Level 1 : High Level	Pull-up
2	R	Px.2ILEV : Px.2 Input Level bit 0 : Low Level 1 : High Level	Pull-up
1	R	Px.1ILEV : Px.1 Input Level bit 0 : Low Level 1 : High Level	Pull-up
0	R	Px.0ILEV : Px.0 Input Level bit 0 : Low Level 1 : High Level	Pull-up

GPIO Pull-up Status Registers (PxPUS)

Address : 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	Px.yUP : Px.y Pull-up Status bit 0 : Pull-up Disable 1 : Pull-up Enable	0xFF

GPIO Pull-up Enable Registers (PxPUEN)

Address : 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7PUEN : Px.7 Pull-up enable bit	-
6	W	Px.6PUEN : Px.6 Pull-up enable bit	-
5	W	Px.5PUEN : Px.5 Pull-up enable bit	-
4	W	Px.4PUEN : Px.4 Pull-up enable bit	-
3	W	Px.3PUEN : Px.3 Pull-up enable bit	-
2	W	Px.2PUEN : Px.2 Pull-up enable bit	-
1	W	Px.1PUEN : Px.1 Pull-up enable bit	-
0	W	Px.0PUEN : Px.0 Pull-up enable bit	-

*** Pull-up enable bit

0 : No effect

1 : Set to pull-up the corresponding bit in the PxPUS registers

GPIO Pull-up Disable Registers (PxPUDIS)

Address : 0xFFFF_301C / 0xFFFF_305C / 0xFFFF_309C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	Px.7PUDIS : Px.7 Pull-up disable bit	-
6	W	Px.6PUDIS : Px.6 Pull-up disable bit	-
5	W	Px.5PUDIS : Px.5 Pull-up disable bit	-
4	W	Px.4PUDIS : Px.4 Pull-up disable bit	-
3	W	Px.3PUDIS : Px.3 Pull-up disable bit	-
2	W	Px.2PUDIS : Px.2 Pull-up disable bit	-
1	W	Px.1PUDIS : Px.1 Pull-up disable bit	-
0	W	Px.0PUDIS : Px.0 Pull-up disable bit	-

*** Pull-up disable bit

0 : No effect

1 : Set to pull-up the corresponding bit in the PxPUS registers

GPIO Rising Edge Detect Registers (PxRED)

Address : 0xFFFF_3020 / 0xFFFF_3060 / 0xFFFF_30A0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	Px.7RED : Px.7 Rising Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	Px.6RED : Px.6 Rising Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	Px.5RED : Px.5 Rising Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	Px.4RED : Px.4 Rising Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	Px.3RED : Px.3 Rising Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	Px.2RED : Px.2 Rising Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	Px.1RED : Px.1 Rising Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	Px.0RED : Px.0 Rising Edge Detect bit 0 : Disable 1 : Enable	0

*** When Rising Edge and Falling Edge are set at the same time, it becomes Any Edge mode.

GPIO Falling Edge Detect Registers (PxFED)

Address : 0xFFFF_3024 / 0xFFFF_3064 / 0xFFFF_30A4

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	Px.7FED : Px.7 Falling Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	Px.6FED : Px.6 Falling Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	Px.5FED : Px.5 Falling Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	Px.4FED : Px.4 Falling Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	Px.3FED : Px.3 Falling Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	Px.2FED : Px.2 Falling Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	Px.1FED : Px.1 Falling Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	Px.0FED : Px.0 Falling Edge Detect bit 0 : Disable 1 : Enable	0

*** When Rising Edge and Falling Edge are set at the same time, it becomes Any Edge mode.

GPIO Edge Detect Status Registers (PxEDS)

Address : 0xFFFF_3028 / 0xFFFF_3068 / 0xFFFF_30A8

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	Px.7EDS : Px.7 Edge Detect Status bit	0
6	R/W	Px.6EDS : Px.6 Edge Detect Status bit	0
5	R/W	Px.5EDS : Px.5 Edge Detect Status bit	0
4	R/W	Px.4EDS : Px.4 Edge Detect Status bit	0
3	R/W	Px.3EDS : Px.3 Edge Detect Status bit	0
2	R/W	Px.2EDS : Px.2 Edge Detect Status bit	0
1	R/W	Px.1EDS : Px.1 Edge Detect Status bit	0
0	R/W	Px.0EDS : Px.0 Edge Detect Status bit	0

*** Edge Detect Status bit
0 : No edge detect has occurred on pin
1 : Edge detect has occurred on pin

*** Status bits are cleared by writing a one to them.
*** Writing a zero to a status bit are no effect.

GPIO Open Drain Mode Control Registers (PxODM)

Address : 0xFFFF_302C / 0xFFFF_306C / 0xFFFF_30AC

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	Px.yOD : Px.y Open Drain Mode Setting bit 0 : Normal CMOS Output Mode 1 : Open Drain Mode	0

10 WATCHDOG TIMER

The Watchdog Timer is responsible for returning to a normal state when the CPU does not operate normally due to system errors, non-responsive devices, or noise.

When watchdog timer is enabled, watchdog reset occurs when WDTCNT value becomes '0' by decrementing by '1' from the value set in WDTCNT.

When watchdog reset occurs, the state of watchdog reset is stored in WDTST bit.

Once the Watchdog Timer is set, the WDTCNT should be reset periodically so that the Watchdog Counter value does not become '0' in order to prevent Watchdog Reset from taking place.

If the WDTMOD bit is set to Interrupt mode, watchdog reset does not occur and an interrupt is generated to indicate that the value set in WDTCNT is 0.

10.1 Watchdog Timer Control Registers

Watchdog Timer Control Register (WDTCTRL)

Address : 0x8002_0400

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
4	R	WDTST : Watchdog timer status bit When watchdog timer is reset mode, 0 : No watchdog reset 1 : Watchdog reset When watchdog timer is interrupt mode, 0 : No watchdog interrupt 1 : Watchdog interrupt Clear at read	0
3 : 2	R	Reserved	-
1	R/W	WDTMOD : Watchdog timer mode select bit 0 : Reset mode 1 : Interrupt mode	0
0	R/W	WDTEN : Watchdog timer enable bit 0 : Disable 1 : Enable	0

Watchdog Timer Counter Value Register (WDTCNT)

Address : 0x8002_0404

Bit	R/W	Description	Default Value
31 : 0	R/W	Watchdog timer counter 32-bit value. Down-counter	0xFFFF_FFFF

11 TIMERS

Includes 3 channels of 16-bit Timer / Counter with Timer / Counter, Capture, PWM, and Output Compare.

Key Features

- 15-bit Pre-scale
- 16-bit Timer/Counter
- 16-bit Capture
- 16-bit PWM
- 16-bit Output Compare
- 16-bit Timer Counter Wave-Out

11.1 15-bit Prescaler with clock source selection

The pre-scaler selects the input received from the outside via the system clock and the external clock pin through the CLKSEL bit, generates a 1/2 ~ 1/32768 times clock through the 15-bit Pre-scaler, . The Timer / Counter selects the clock divided by the pre-scaler to drive the 32-bit counter.

If the precise phase of the clock divided by the pre-scaler is needed, it is used after initializing the pre-scaler counter through the CNTCLR bit in the TPxCON register.

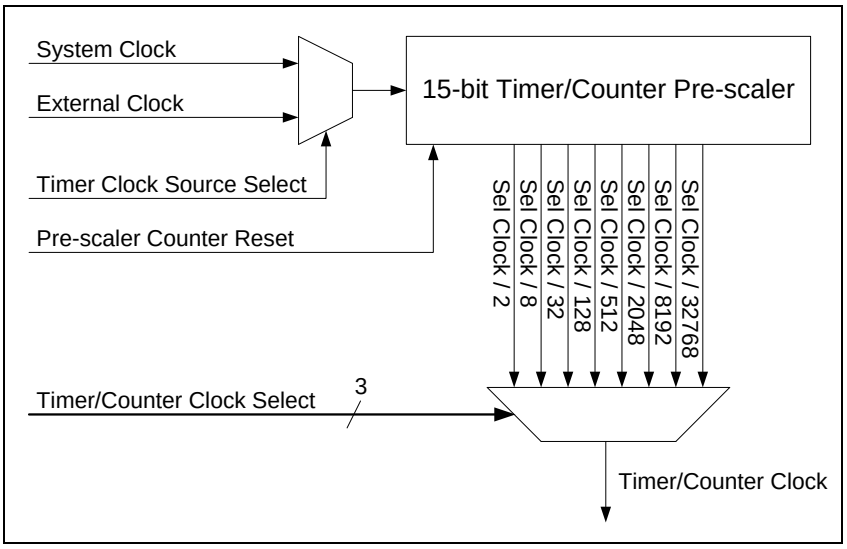


Figure 11-1 Pre-scaler Block Diagram

11.2 Timer/Counter

Using the clock divided by the pre-scaler, the counter value is incremented by "1" every clock from the initial value of 0x0, and when it reaches the Timer Counter register value set by the user.

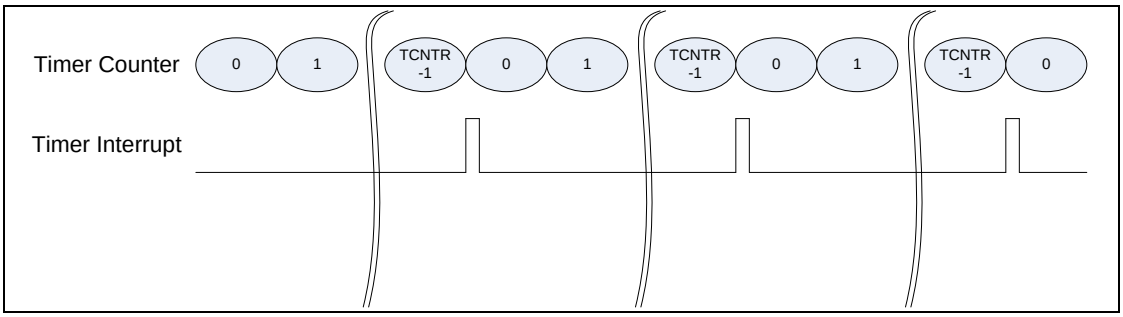


Figure 11-2 Timer Operation

The Timer period is determined by the selected clock, Pre-scaler and Timer Counter.

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Freq.} \times \frac{1}{\mathrm{Pre}-scaler\ \ Factor} \times (TMCNT)\ [\mathrm{sec}] \qquad \{\mathrm{Pre}-scaler\ \ Factor \geq 3\}$$

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Freq.} \times \frac{1}{\mathrm{Pre}-scaler\ \ Factor} \times (TMCNT+1)\ [\mathrm{sec}] \qquad \{\mathrm{Pre}-scaler\ \ Factor < 3\}$$

Timer Period Example :

- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Timer Counter Value (TMCNT) : 1000

=> 1/12MHz X 1024 X 1000 = 85.333msec = 11.718Hz

The registers that must be set to operate with the Timer Counter are:.

- TPxCON : Determine the clock input of the pre-scaler and clear the pre-scaler as needed.
- TMxCON's TMOD : Set the Timer Counter mode.
- TMxCON's WAVE : Determines whether to output the clock generated by the cycle of the timer counter.
- TMxCON's PFSEL : Determine the Clock to be used by the Timer Counter.
- TMxCON's TMEN : Enable Timer Counter.
- TMxCNT : Determine the maximum counter value of the Timer Counter.

The Timer Counter operates in the following order.

- TPxCON setting
- TMxCNT setting
- TMxCTRL setting
- TPxCTRL's CNTCLR bit setting as required

11.3 Pulse Width Modulation (PWM)

PWM is a controller for outputting pulse signals of programmable duty and period.

It operates through the clock set by the Pre-scaler and it repeats the count in the cycle of the PWM Period register value and outputs the waveform of the type set by the user.

The output pulse of the PWM is inverted every time the value of the 32-bit counter reaches the PWM Duty, PWM Period register value, and the output waveform is generated. The number of PWM output is determined by the PWM Pulse Number register. When the number of pulses reaches the number of output, a PWM interrupt is generated. However, even if PWM interrupt occurs, the PWM output is continuously generated if there is no other setting.

$$PWM\ \ Period = \frac{1}{Clock\ \ Source\ \ Freq.} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$PWM\ \ Period = \frac{1}{Clock\ \ Source\ \ Freq.} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

PWM Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- PWM Period Value(TMxCNT) : 10
- PWM Duty Value : 6

=> 1/12MHz X 1024 X 10 = 0.853msec = 1.171KHz

The registers to be set to operate with PWM are as follows.
- TPxCTRL: Determines the clock input of the pre-scaler and clears the pre-scaler if necessary.
- TMxCTRL's TMOD: Set to PWM mode.
- TMxCTRL's PWML: Determines the start level of the PWM output.
- TMxCTRL's PFSEL: Determines the clock to use in PWM.
- TMxCTRL's TMEN: Enable PWM.
- TMxCNT: Determines the period of the PWM.
- TMxDUT: Determines the PWM duty.
- TMxPUL: Determines the number of PWM pulses. Timer Interrupt occurs when the number of PWM pulses reaches this register value. However, the PWM Pulse continues to be generated without stopping.

PWM operates in the following order.
- TPxCTRL setting
- TMxCNT setting
- TMxDUT setting
- TMxPUL setting
- Set TPxCTRL's CNTCLR as required

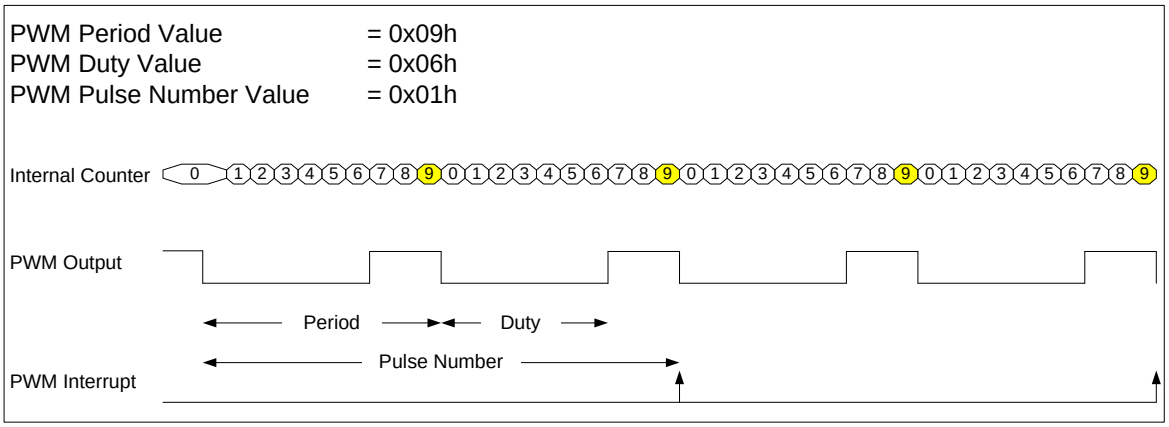


Figure 11-3 PWM Operation

11.4 Capture

The Capture function measures the external input based on the clock set in the Pre-scale.

The external input can measure pulse period of 5 types: Low / High Pulse, Only Low Pulse, Only High Pulse, Falling to Falling Period, and Rising to Rising Period.

When enabling the Timer in Capture mode, the first captured value should be ignored as it is the middle value of the signal change.

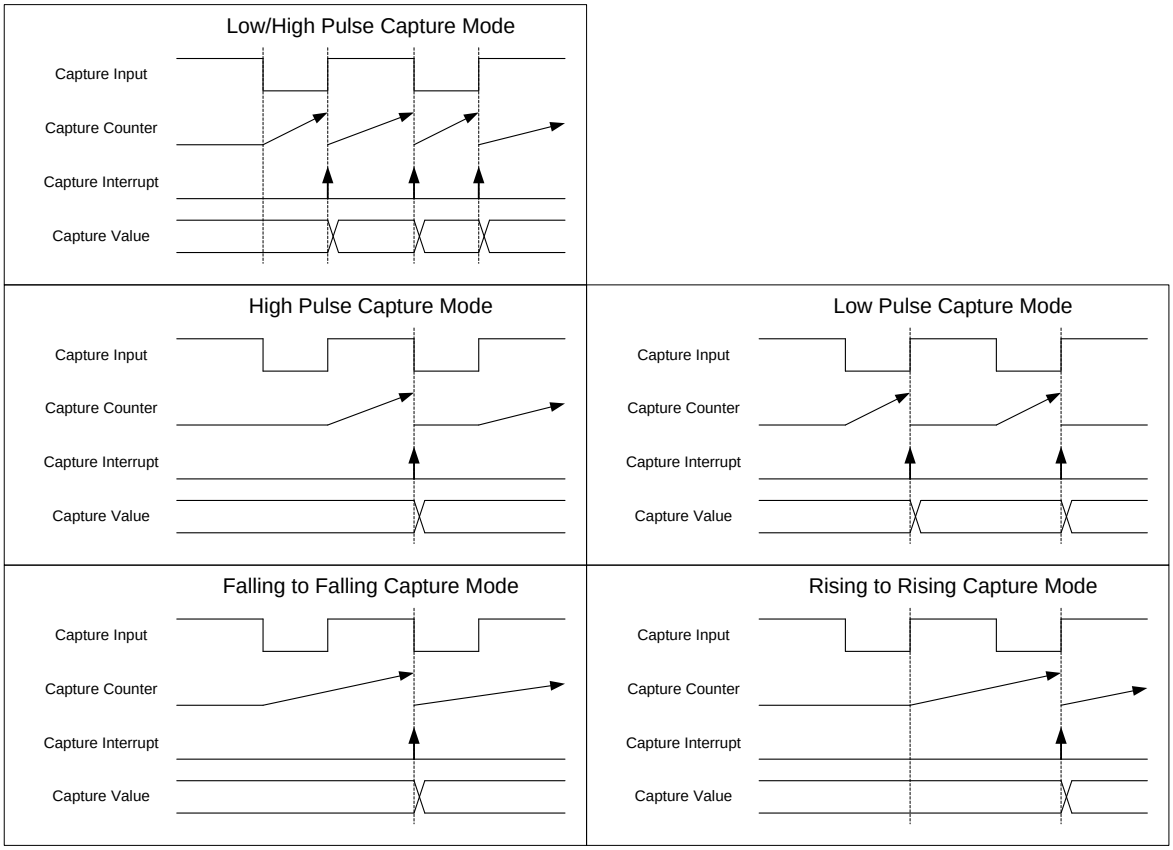


Figure 11-4 Capture Mode Operation

The capture cycle is measured as follows.

$$Capture\ \ Signal\ \ Width\ \ Time = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\mathrm{Pr}e-scaler\ \ Factor} \times (OCA+1)\ \ [\mathrm{sec}]$$

Capture Time Example :

- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Capture Value : 9

=> 1/12MHz X 1024 X 10 = 0.853msec

The registers that must be set to operate in capture mode are:
- TPxCTRL: Determines the clock input of the pre-scaler and clears the pre-scaler if necessary.
- TMxCTRL's TMOD: Set to Capture mode.
- TMxCTRL's CAPMOD: Determines Capture Pulse type.
- TMxCTRL's PFSEL: Determines the clock to use in Capture.
- TMxCTRL's TMEN: Enable Capture.

Capture operates in the following order.
- TPxCTRL setting
- TMxCTRL setting
- Set TPxCTRL's CNTCLR as required
- Read Capture cycle by reading TMxDUT
- Read TMxCTRL's OVST to check for overflow

11.5 Output Compare Mode

Timer Channels 2 and 3 have two Output Compare registers, so you can perform two Output Compare cycles before the timer counter overflows.

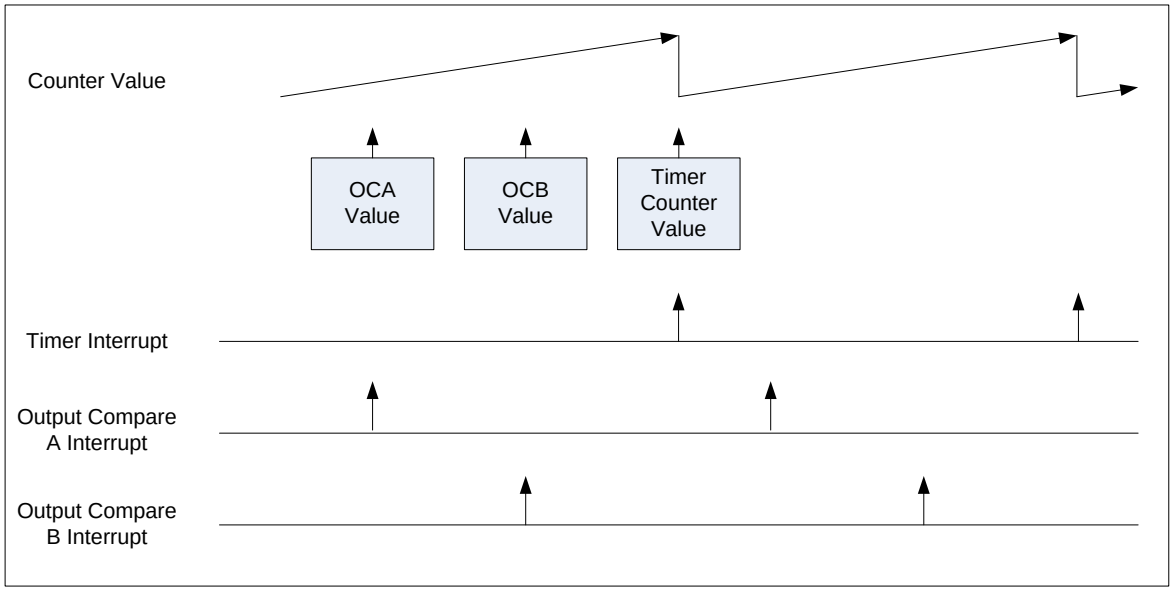


Figure 11-5 Timing Diagram of Output Compare Operation

11.6 Timer Control Registers

Timer Pre-scale Control Registers (TPxCTRL)

Address : 0x8002_0800 / 0x8002_0820 / 0x8002_0840

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
1	R/W	CNTCLR : Pre-scale Counter and Timer Counter Reset When this bit is "1", the Timer Pre-scale and Counter will be reset.	0
0	R/W	CLKSEL : Pre-scale Clock Selection 0 : System clock 1 : CAPx	0

*** CAPx is assigned to each Timer channel.

Timer Control Registers (TMxCTRL)

Address : 0x8002_0804 / 0x8002_0824 / 0x8002_0844

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 14	R/W	TMOD : Timer/Counter Mode 00 : Timer 01 : PWM 1x : Capture	00
13	R/W	OCEN : Output Compare Mode Enable bit for channel 2 and channel 3 0 : Disable 1 : Enable	0
12	R	Reserved	0
11	R/W	OVST : Capture Overflow Status bit Read시 Overflow status bit가 clear된다.	0
10 : 8	R/W	CAPMOD : Capture Mode Selection 00x : Low/High Pulse Capture mode 010 : Low Pulse Capture mode 011 : High Pulse Capture mode 10x : Failing to Failing Period Capture mode 11x : Rising to Rising Period Capture mode	000
7	R	Reserved	-
6	R/W	PWMO : PWM Output One Period Generation 0 : Disable 1 : Enable	0
5	R/W	PWML : PWM Output Start Level 0 : Start Level is Low 1 : Start Level is High	0
4	R	Reserved	-
3 : 1	R/W	PFSEL : Pre-scale Factor Selection 000 : 1/2 001 : 1/8 010 : 1/32 011 : 1/128 100 : 1/512 101 : 1/2048 110 : 1/8192 111 : 1/32768	111
0	R/W	TMEN : Timer/Counter or PWM Enable 0 : Disable 1 : Enable	0

*** PWM Output One Period Generation: When operating in PWM mode, it is a bit that generates only one period. After one cycle occurs, PWM is automatically disabled.

Timer Counter / PWM Period Registers (TMxCNT)

Address : 0x8002_0808 / 0x8002_0828 / 0x8002_0848

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(Timer mode) - Write : Timer Counter Value - Read : Current Up-counter Value (PWM mode) - Read/Write : PWM Period Value	0xFFFF

Capture Counter Registers / PWM Duty Registers / Output Compare A Registers (TMxDUT)

Address : 0x8002_080C / 0x8002_082C / 0x8002_084C

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(Capture mode) - Read : Result value of counting at the sampling period (PWM mode) - Read/Write : PWM Duty Value (Output Compare Mode) - Read/Write : Output Compare A Value - Supported in channel2 and channel3	0xFFFF

*** PWM Duty : First Halt Duty of PWM Pulse

PWM Pulse Count Registers / Output Compare B Registers (TMxPUL)

Address : 0x8002_0810 / 0x8002_0830 / 0x8002_0850

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(PWM mode) - Read/Write : PWM Pulse Number Value (Output Compare Mode) - Read/Write : Output Compare B Value - Supported in channel2 and channel3	0xFFFF

12 UART

The UART is equipped with a general PC and I / O device with RS-232C interface and a 3-channel Universal Asynchronous Receiver / Transmitter (UART) controller with various control functions for serial asynchronous communication.

Key Features

- Compatible with standard 16450/16550 UARTs
- Fully programmable serial-interface protocols
  - 5,6,7,8-bit characters
  - Even, odd or no-parity, stick parity generation and detection
  - 1, 1.5, 2 stop bit generation
  - Baud rate generator
- Line break generation and detection
- False start bit detection
- Prioritized transmit, receive and line status control interrupts
- Independent 16 characters transmit and receive 16Bytes FIFOs
- 3 Ch. UARTs

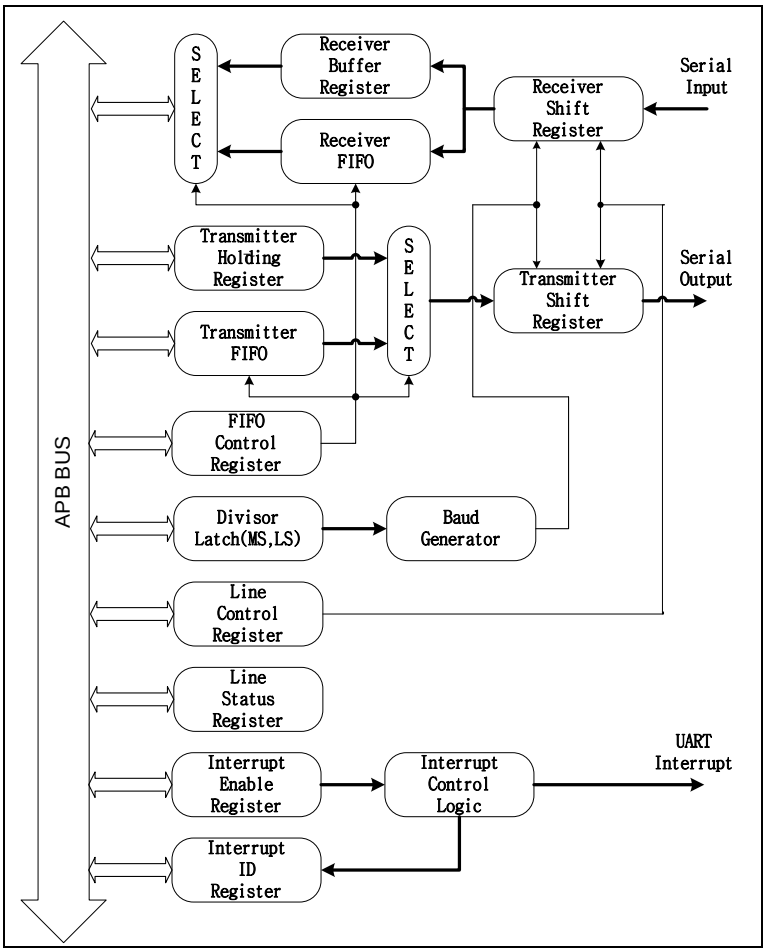


Figure 12-1 UART Block Diagram

12.1 UART Registers Summery

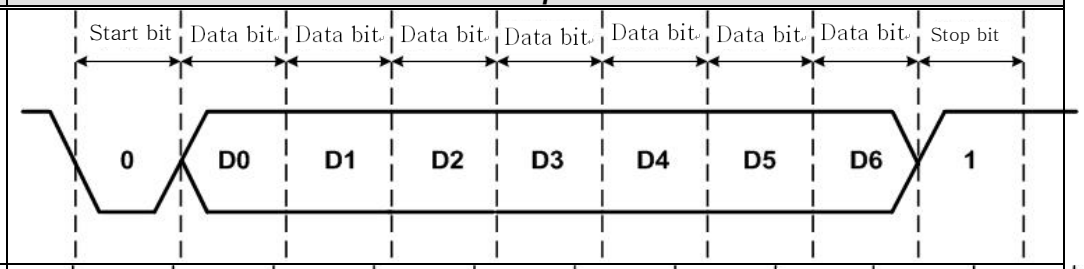
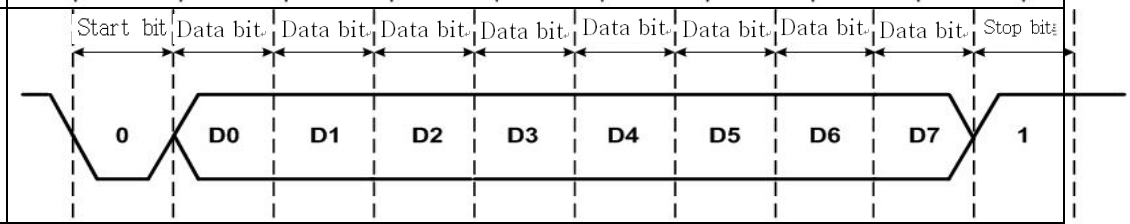
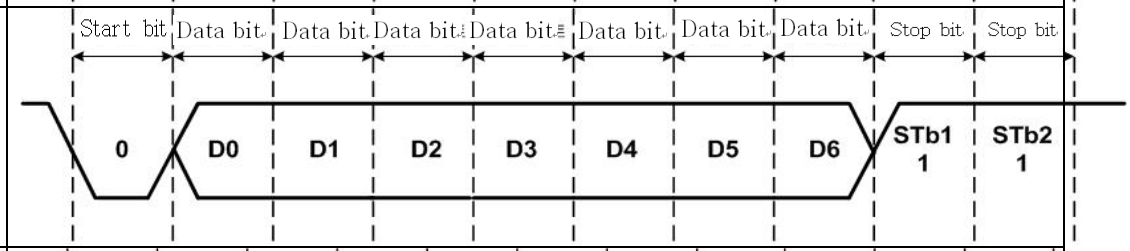
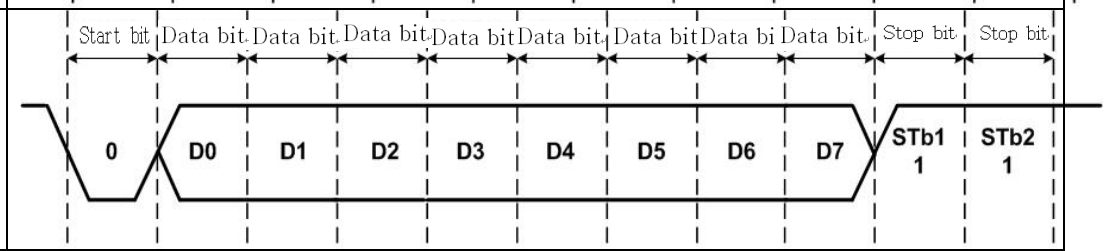
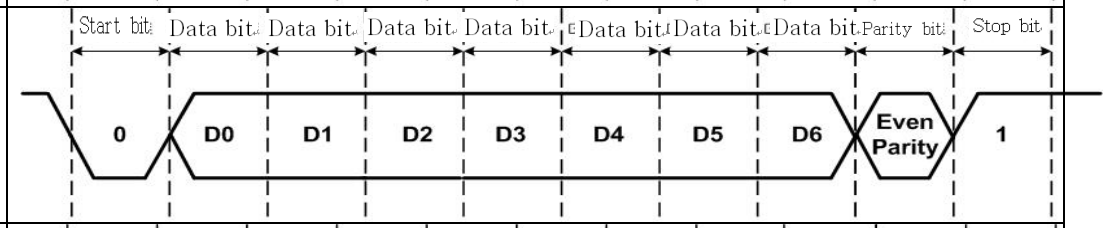
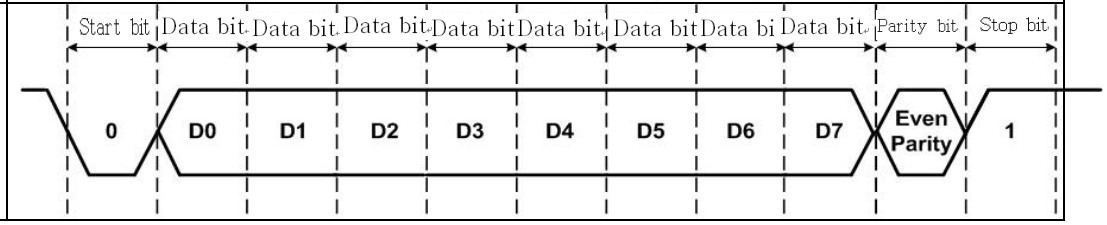
Table 12.1-1 UART Register Summery

Bit No.	DLAB = 0 0x00	DLAB = 0 0x00	DLAB = 0 0x04	DLAB = 0 0x08	DLAB = X 0x08	DLAB = X 0x0C	DLAB = X 0x14	DLAB = 1 0x00	DLAB = 1 0x04
	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Ident. Register	FIFO Control Register	Line Control Register	Line Status Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	LSR	DLL	DLM
	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Ready	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit 0	RCVR FIFO Reset	Word Length Select Bit 1	Overrun Error	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit 1	XMIT FIFO Reset	Number of Stop Bits	Parity Error	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	0	Interrupt ID Bit 2	0	Parity Enable	Framing Error	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Break Interrupt	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Transmitter Holding Register	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled	RCVR Trigger(LSB)	Set Break	Transmitter Empty	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled	RCVR Trigger(MSB)	Divisor Latch Access Bit (DLAB)	Error in RCVR FIFO	Bit 7	Bit 7

* DLAB = LCR[7](Divisor Latch Access Bit)
* FIFO Control Register :
  - DLAB = 0 : Register Write
  - DLAB = 1 : Register Read
* Addresses 0x10 (0x30), 0x18 (0x38), 0x1C (0x3C) are reserved for compatibility with the 16550 UART standard.

12.2 Serial Data Format

In UART, UART communication serial data format can be changed by register setting of ULCRn [4: 0] bit. The following table describes the data formats that can be changed by register setting of ULCRn [4: 0] bits.

ULCRn[4:0]	Description
00010 No Parity / 1 Stop bit / 7 Data bit	
00011 No Parity / 1 Stop bit / 8 Data bit	
00110 No Parity / 2 Stop bit / 7 Data bit	
00111 No Parity / 2 Stop bit / 8 Data bit	
11010 Even Parity / 1 Stop bit / 7 Data bit	
11011 Even Parity / 1 Stop bit / 8 Data bit	

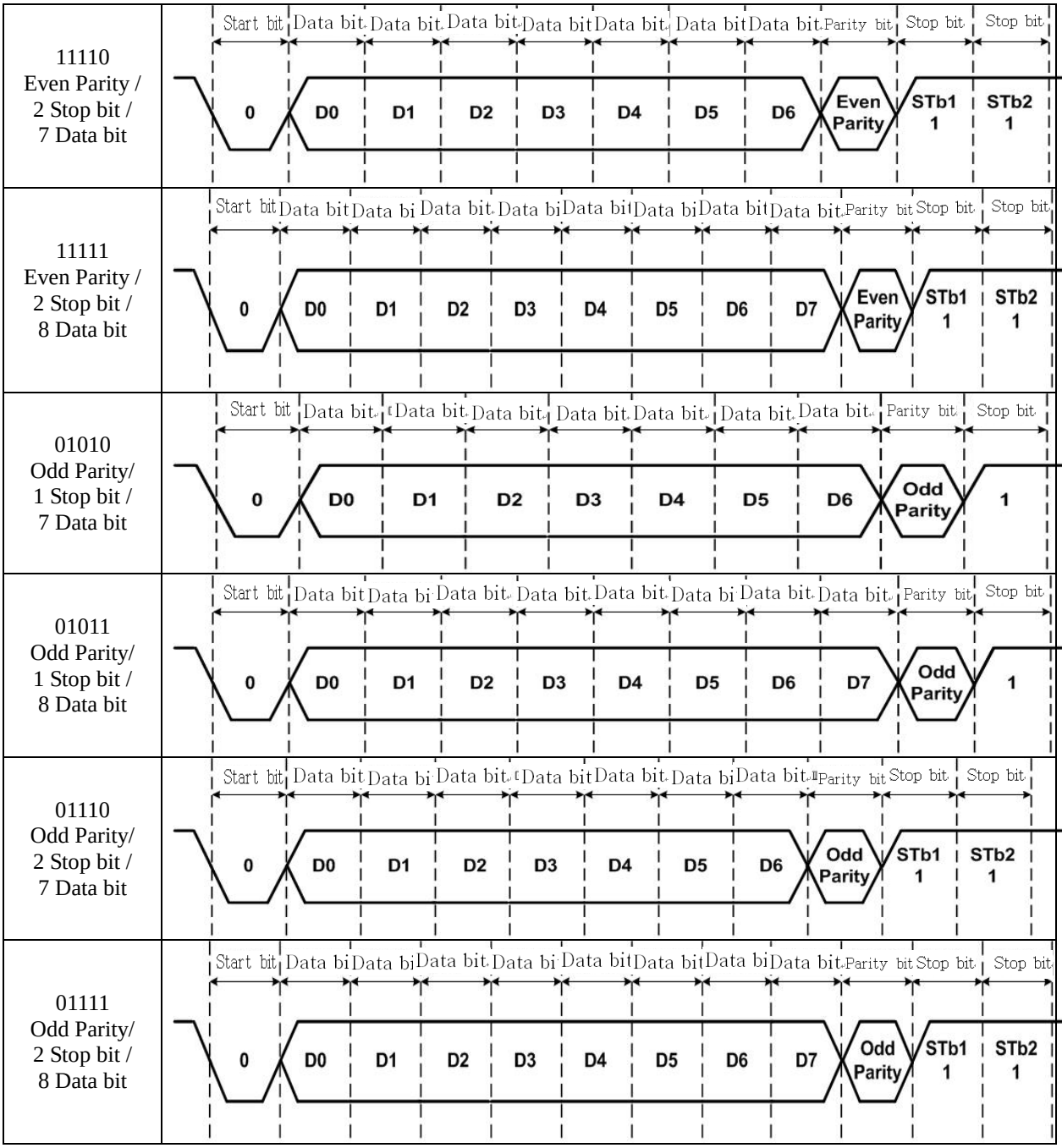
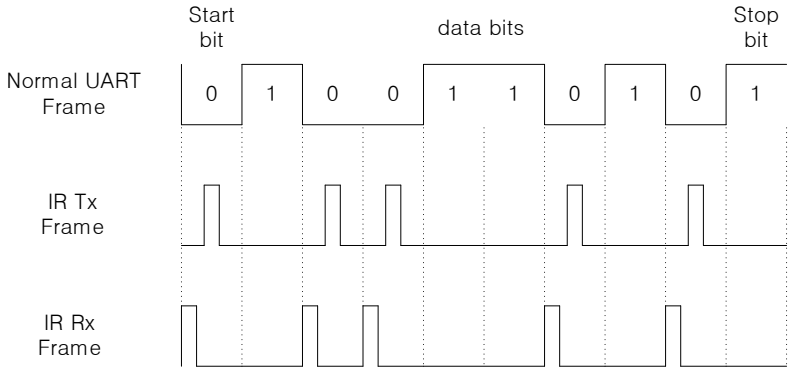


Figure 12-2 UART LCR Register Setting and Serial Data Format

12.3 IRDA Mode

It supports IrDA 1.0. The low speed IR frame below 115.2Kbit / s is compatible with UART frame as shown below. This UART has the function to decode or encode the IR frame through the built-in hardware module in the IRDA mode.



12.4 UART Baud Rate

TX / RX Baud Rate is calculated by the following equation.

$$UART\ \ Baud\ \ Rate = \frac{f_{PCLK}}{16\ \times\ UDL}$$

UART Divisor Latch Value (UDL) = UDLM[7:0] << 8 + UDLL[7:0]

Table 12.4-1 UART Baud Rate

f_{PCLK} (MHz)		1.024	2.048	5.6448	11.2896	24.0	48.0
2400 bps	UDL	27	53	147	294	625	1250
	ERR(%)	1.23	0.63	0.00	0.00	0.00	0.00
4800 bps	UDL	-	27	74	147	313	625
	ERR(%)	-	1.23	0.68	0.00	0.16	0.00
9600 bps	UDL	-	-	37	74	156	313
	ERR(%)	-	-	0.68	0.68	0.16	0.16
14400 bps	UDL	-	9	25	49	104	208
	ERR(%)	-	1.23	2.00	0.00	0.16	0.16
19200 bps	UDL	-	-	18	37	78	156
	ERR(%)	-	-	2.08	0.68	0.16	0.16
38400 bps	UDL	-	-	9	18	39	78
	ERR(%)	-	-	2.08	2.08	0.16	0.16
57600 bps	UDL	-	-	6	12	26	52
	ERR(%)	-	-	2.08	2.08	0.16	0.16
115200bps	UDL	-	-	3	6	13	26
	ERR(%)	-	-	2.08	2.08	0.16	0.16

*** Stability of UART operation can not be guaranteed when ERR is above 2.2%.

12.5 UART Control Registers

UART Channel Receiver Buffer Registers (UxRB)

Address : 0x8002_0C00 / 0x8002_0C20 / 0x8002_0C40 / 0x8002_0C60

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	R	Receive Buffer Data	-

*** Access is possible when DLAB is "0".

UART Channel Transmitter Holding Registers (UxTH)

Address : 0x8002_0C00 / 0x8002_0C20 / 0x8002_0C40 / 0x8002_0C60

Bit	R/W	Description	Default Value
31: 8	W	Reserved.	-
7 : 0	W	Transmit Holding Data	-

*** Access is possible when DLAB is "0".

UART Channel Interrupt Enable Registers (UxIE)

Address : 0x8002_0C04 / 0x8002_0C24 / 0x8002_0C44 / 0x8002_0C64

Bit	R/W	Description	Default Value
31: 3	R	Reserved.	-
2	RW	RLSIEN : Receiver Line Status Interrupt Enable bit 0 : Disable 1 : Enable	0
1	RW	THEIEN : Transmitter Holding Empty Interrupt Enable bit 0 : Disable 1 : Enable	0
0	RW	RDAIEN : Received Data Available Interrupt Enable bit 0 : Disable 1 : Enable	0

*** Access is possible when DLAB is "0".

UART Channel Interrupt Identification Register (UxII)

Address : 0x8002_0C08 / 0x8002_0C28 / 0x8002_0C48 / 0x8002_0C68

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	R	FIFOST : FIFOs Enabled Status bit. 00 : not in FIFO mode 11 : FIFO mode	00
5 : 4	R	Reserved	0
3 : 1	R	INTID : UART Interrupt ID (Note, UART Interrupt Control Function)	000
0	R	INTP : UART Interrupt Pending bit When this bit is a logic 1, no interrupt is pending	1

*** Access is possible in Read Mode only when DLAB is "0".

Table 12.5-1 UART Interrupt Control Function

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Condition
Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters have been removed from or input to the RCVR FIFO during the last 4 Char. times, and there is at least 1 Char. in it during this Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register

UART Channel FIFO Control Register (UxFC)

Address : 0x8002_0C08 / 0x8002_0C28 / 0x8002_0C48 / 0x8002_0C68

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	RW	RFTL : Receiver FIFO Trigger Level 00 : 1 Byte 01 : 4 Byte 10: 8 Byte 11 : 14 Byte	00
5 : 3	R	Reserved	-
2	RW	XFR : XMIT FIFO Reset When XFR is "1", all data in the XMIT FIFO are reset. However, the data in the shift register is not reset.	0
1	RW	RFR : RCVR FIFO Reset When RFR is "1", all data in the RCVR FIFO is reset, but the data in the shift register is not reset.	0
0	RW	FIFOEN : FIFO Enable Bit 0 : 16450 UART Mode 1 : Enables FIFO	0

*** When the DLAB is "0", it is the Write Mode, and when the DLAB is "1", it is the Read Mode.

UART Channel Line Control Register (UxLC)

Address : 0x8002_0C0C / 0x8002_0C2C / 0x8002_0C4C / 0x8002_0C6C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	RW	DLAB : Divisor Latch Access Bit When DLAB is "1", Read / Write of Divisor Latch Registers and Read of FIFO Control Register are possible.	0
6	RW	SB : Set Break When SB is "1", Logic "0" is output to the Serial Data Output. SB does not affect internal Transmitter Logic, but only affects Serial Output.	0
5	RW	SP : Stick Parity 0 : Disables Stick Parity 1 : When PEN, EPS, SP is "1", Parity Bit "0" When PEN, SP is "1" and EPS is "0", Parity Bit "1"	0
4	RW	EPS : Even Parity Select 0 : Select Odd Parity 1 : Select Even Parity	0
3	RW	PEN : Parity Enable Bit 0 : Disables Parity 1 : Enables Parity	0
2	RW	STB : Number of Stop Bit 0 : 1 Stop bit 1 : 2 Stop bits(If you have selected 5 Bits / Character in the WLS Bit, it will have 1.5 Stop bits.)	0
1 : 0	RW	WLS : Word Length Select 00 : 5 Bits/Character 01 : 6 Bits/Character 10 : 7 Bits/Character 11 : 8 Bits/Character	00

UART Channel Line Status Register (UxLS)

Address : 0x8002_0C14 / 0x8002_0C34 / 0x8002_0C54 / 0x8002_0C74

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	R	EIRF : Error in RCVR FIFO EIRF is always "0" if it is not in FIFO mode. In FIFO mode, EIRF is set to "1" if any of OE, PE, FE, or BI is set to "1" in the RCVR FIFO. EIRF is cleared ("0") when the LSR register is read if there are no consecutive errors in the FIFO.	0
6	R	TEMP : Transmitter Empty When not in FIFO mode, TEMT becomes "1" when both Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are Empty. Clear if there is data in THR or TSR. In FIFO mode, TEMT is "1" when both the Transmitter FIFO and TSR are Empty.	1
5	R	THRE : Transmitter Holding Register Empty In the case of FIFO mode, THRE becomes "1" when THR data is transferred to TSR and Empty, and THR can write new data for transmission. In FIFO mode, THRE becomes "1" when Transmit FIFO is Empty, and cleared when at least one Byte is written to Transmit FIFO. If THRE interrupt (ETHREI) is "1" and THRE is "1", an interrupt occurs.	1
4	R	BINT : Break Interrupt : BI is "1" when the input data to be received is "0" during Full-word transfer time. Full-word transfer time refers to the total time for Start, Data, Parity and Stop bit transfer. In FIFO mode, this error is applied to each byte in the FIFO, and a "0" is written to the FIFO when BI occurs. Clear when CPU reads LSR.	0
3	R	FERR : Framing Error FE is "1" when the input data received does not have a valid Stop bit. In FIFO mode, this error is applied to each Byte in the FIFO. Clear when CPU reads LSR.	0
2	R	PERR : Parity Error PE is "1" when the input data received is not the same as the parity bit selected by the LCR register. In FIFO mode, this error is applied to each Byte in the FIFO. Clear when CPU reads LSR.	0
1	R	OERR : Overrun Error OE is used when the FIFO mode is not used, before the data in the RBR is read & Quot; 1 & quot; In FIFO mode, this is "1" when the FIFO is full and a new Full-word is input to the Receiver Shift Register (RSR). In this case, the RSR is continuously updated with new data, but is not transferred to the FIFO. Clear when CPU reads LSR.	0
0	R	DRDY : Data Ready DR becomes "1" when the received data is written to RBR or FIFO. Cleared when all data in the RBR or FIFO is read by the CPU.	0

UART Channel Divisor Latch LSB Register (UxDLL)

Address : 0x8002_0C00 / 0x8002_0C20 / 0x8002_0C40 / 0x8002_0C60

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Least Significant Byte	0x00

*** Access is possible when DLAB is "1".

UART Channel Divisor Latch MSB Register (UxDLM)

Address : 0x8002_0C04 / 0x8002_0C24 / 0x8002_0C44 / 0x8002_0C64

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Most Significant Byte	0x00

*** Access is possible when DLAB is "1".

UART IRDA Mode Register (UxIRM)

Address : 0x8002_0C78

Bit	R/W	Description	Default Value
31: 6	R	Reserved.	-
5	RW	IrDA Rx Polarity Inversion	0
4	RW	IrDA Rx Decoding Enable 0 : not decoding 1 : decoding the IR Frame	0
3 : 2	R	Reserved	00
1	RW	IrDA Tx Polarity Inversion	0
0	RW	IrDA Tx Encoding Enable 0 : not encoding 1 : encoding the UART frame	0

13 SPI (SERIAL PERIPHERAL INTERFACE)

The SPI exchanges data with external devices or other CPUs over a synchronous serial bus. The SPI is compatible with Motorola M68HC11, M68HC05 and MC68HC16 series of SPIs and can perform full duplex 3-wire transmission or Half duplex 2-wire.

8-byte FIFO is built in for high-speed SPI transmission, so that it can be performed without imposing a burden on the CPU even in transmission of Mbps speed.

SPI supports both Master Mode and Slave Mode.

Key Features

- Full duplex mode. Three-wired synchronous Transfer
- Master or Slave Operation
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-master mode fault protection capability
- 8Bytes FIFO

Compatibility with most synchronous serial peripherals is achieved through selection of clock polarity and selection of two clock protocols in the clock control circuit. When the SPI is set to Master, you can create 256 different serial clocks in software.

In the SPI, the data transmission operation and the data reception operation are simultaneously performed. Sampling and shifting of information in both serial data lines is synchronized by a serial clock line. Slave The individual selection of SPI devices can be done via the slave selection line. An unselected slave device does not affect the operation of the SPI bus. In Master SPI devices, the slave select line can be used to indicate multiple master bus collisions.

The error detection circuit is used for connection between processes. If data is written to the serial shift register during transmission, a write conflict occurs. Multiple master mode failure detection disables output drivers when more than one CPU tries to become a bus master at the same time.

13.1 SPI Registers Summery

SPI Control Register (SPICTRL): The SPI Control Register contains the parameters related to the SPI settings. This register can be read and written at any time.

SPI Baud Register (SPIBR): The SPI baud register sets the baud rate for creating SCK. .

SPI Status Register (SPISTAT): The SPI Status Register contains SPI status information. The SPI can only set the value of these register bits. The CPU reads the status register to check the current SPI status.

SPI Data Register (SPIDATA): The SPI data register is used for data transmission and reception on the serial bus. TX data register and RX buffer register. Writing is immediately written to the TX data register. After byte or word transfer, the SPIF status bits of the master and slave devices are set.

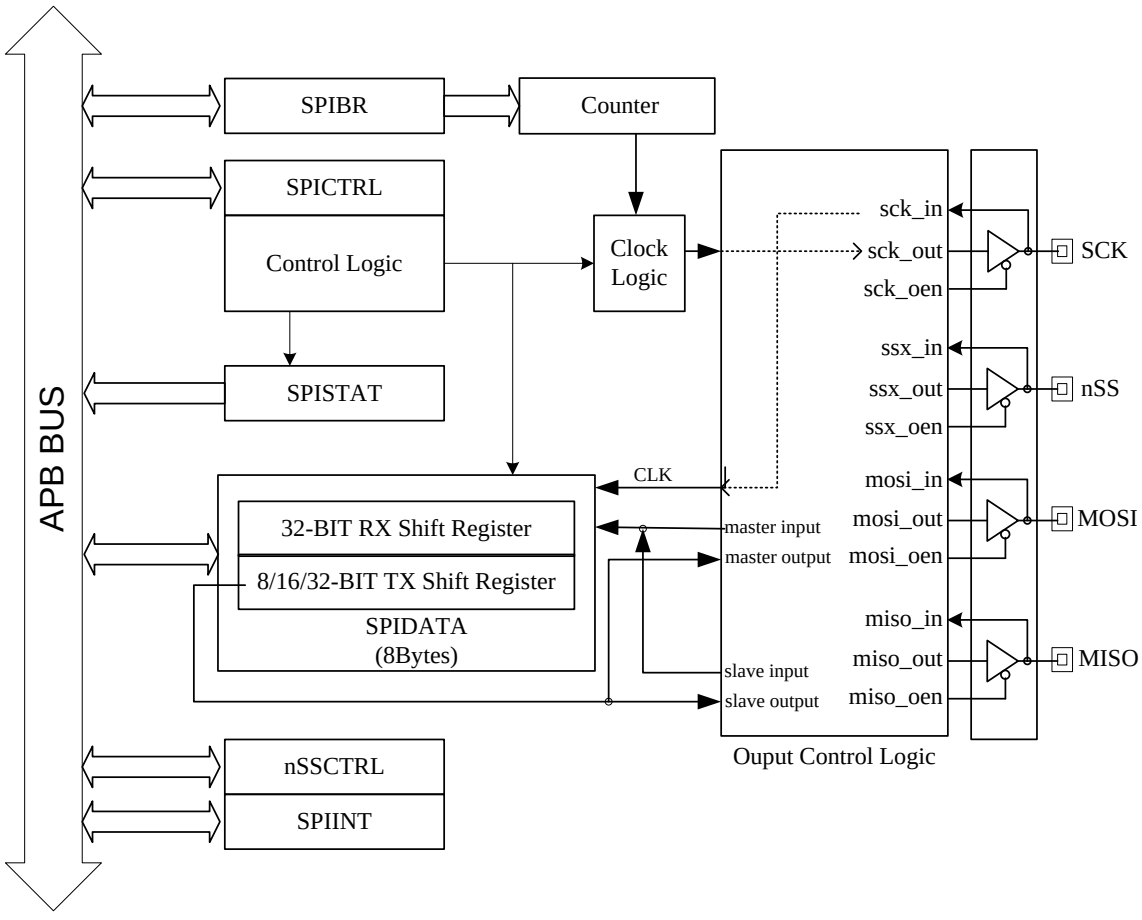


Figure 13-1 SPI Block Diagram

13.2 SPI Pins

SPI has MISO, MOSI, SCK, nSS, and four bidirectional pins. The WOMP bit in the SPI control register determines the Open Drain output or CMOS output for each pin's output operation.

The master or slave operation is determined by the MSTR bit in the SPI control register and the operation of the pin is determined accordingly.

Table 13.2-1 SPI Pin Functions

Pin Name	*Mode*	*Function*
Master in, slave out(MISO)	Master	Provides serial data input to the SPI
	Slave	Provides serial data output from the SPI
Master out, slave in (MOSI)	Master	Provides serial output from the SPI
	Slave	Provides serial input to the SPI
serial clock(SCK)	Master	Provides clock output from the SPI
	Slave	Provides clock input to the SPI
Slave select(nSS)	Master	Output : Selects slave devices
	Slave	Input : chip select for SPI

13.3 SPI Operating Modes

SPI operates in Master or Slave mode. Master mode is used when the CPU is responsible for data transfer. Slave mode is used when serial transfer to the CPU is performed by an external device. The master or slave operation is selected by the MSTR bit in the control register.

Master Mode

Master mode operation is selected by setting the MSTR bit of SPICTRL. In Master mode, it is possible to initialize the serial transmission and does not respond to the external initialized transmission.

To use the SPI in Master mode, proceed as follows.

In Master mode, the MISO pin is used as the serial data input and the MOSI pin is used as the serial data output. Depending on the specific application, one or both may be required.

Assign the values of BAUD, CPHA, CPOL, SIZE, MSBF, and WOMP to the SPICTRL register. Set MSTR bit for master operation. Set the SPIEN bit to enable the SPI.
Enable the slave device.
Write the appropriate data into the SPIDATA register to start the transmission.

The SPI sets the SPIF flag of the SPISTAT register to the H / W level when the transfer is completed. When SPIF is applied, an interrupt request is generated. When SPIF is set and the SPISTAT register is read and the SPIDATA register is written or read, the SPIF flag is

automatically cleared.

Data transfer is synchronized with an internally generated serial clock (SCK). The CPHA and CPOL bits in the SPICTRL register control the phase and polarity of the clock. The SCK edge where the CPU sends data from the MOSI pin and the SCK edge that latches the data coming through the MISO pin are determined by CPHA and CPOL.

Slave Mode

When the MSTR bit in the SPICTRL register is set to "0", it operates in the slave mode. In Slave mode, the SPI can not initiate a serial transfer. Transmission is initiated by an external bus master. Slave mode is especially used on multiple Master SPI buses. Only one device at a given time can be the bus master.

In Slave mode, the MISO pin is used for serial data output and the MOSI pin is used for serial data input. Depending on the particular application, both or only one pin is required. SCK is the input serial clock. When nSS is applied, it is selected as Slave.

Write to the data register for data transfer. In slave mode, SCK, MOSI, and nSS are inputs and MISO is an output.
Writes values to the control registers to set CPHA, CPOL, SIZE, MSBF, and WOMP. Slave operation is selected by clearing the MSTR bit. Enable SPI by setting SPIEN. In slave mode devices, the value of BAUD does not affect SPI operation.

When SPIEN is set and MSTR is cleared, the "Low" state of the nSS pin input initiates the Slave mode operation. The nSS pin is used only as an input.

After byte or word transfer of data, the SPI sets the SPIF flag. If the SPIE bit in the control register is set, an interrupt request occurs when SPIF is applied.

The transmission is synchronized with the externally generated SCK. CPHA and CPOL determine whether the slave CPU latches the data coming through the MOSI pin or the edge of the clock of the data going through the MISO pin.

13.4 SCK Phase and Polarity Control

The two bits of the control register determine the phase and polarity of SCK. The clock polarity (CPOL) bit selects the polarity of the clock (High or Low). The clock phase bit CPHA selects one of two transmission types that affect the transmission timing. The phase and polarity of the clock must be the same for both master and slave. In some cases, the Master device can send and receive data to and from slave devices by changing the phase and polarity between transfers. This flexibility of the SPI allows direct connection to almost all synchronous serial peripherals.

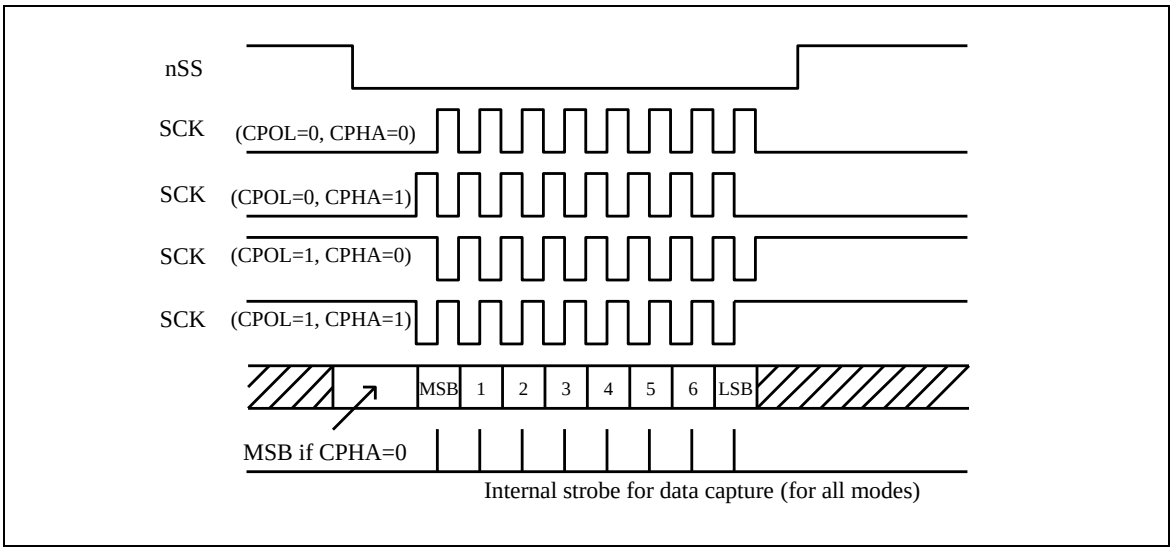


Figure 13-2 SCK Phase and Polarity

13.5 Data Transfer Timing

1Byte data transmission timing diagram is shown in mode where CPHA = '0' and MSB start. The two types of waveforms of SCK are shown. One is a CPOL of '0' and the other is a CPOL of '1'. Since the master and slave are directly connected to the SCK, MISO and MOSI pins, this timing diagram can be viewed either as a master timing diagram or as a slave timing diagram. The MISO signal is the output from the slave and the MOSI signal is the master's output signal. The nSS signal is the chip select signal to the slave.

When data is written to SPDR when it is Master, transfer is initialized. The slave initializes the transmission when nSS is falling edge. The SCK signal remains inactive until the half of the first SCK cycle. The SPIF bit indicating the completion of transmission is set at the end of the eighth SCK cycle. When CPHA = '0', nSS is low and becomes Inactive (High) within a short time after transferring 1 byte. The slave writes a value to the data register when nSS is low, causing a write collision error.

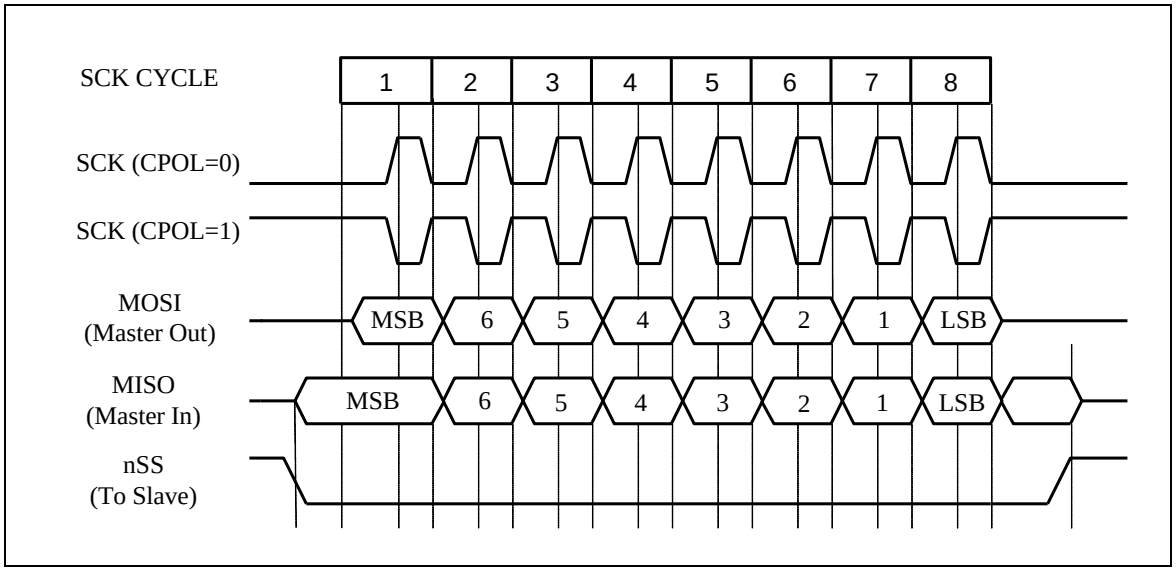


Figure 13-3 Transfer Timing when CPHA = '0'

The timing diagram(Figure 13-4) shows that the the SCK is inactive at the last 8th half cycle in case of CPHA='1'. The SPIF bit is set at the end of the eighth SCK cycle. Since the last edge occurs in the middle period of the 8th SCK cycle, the slave completes the reception after sampling the last data in the middle of the 8th SCK cycle. The nSS maintains low enough for a period of time after completion of transmission of 1 byte. Therefore, if the CPU polls the transmission status and continuously transmits it, the status remains low.

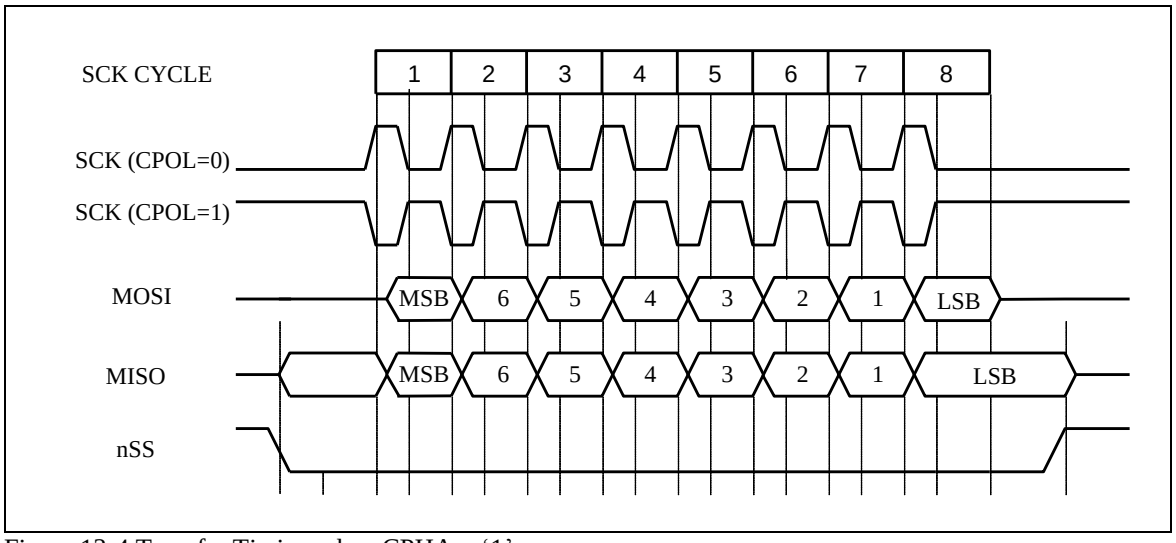


Figure 13-4 Transfer Timing when CPHA = '1'

13.6 SPI Serial Clock Baud Rate

The SPI baud rate can be set by storing a value from 1 to 255 in the SPBR register.

Since it accepts the SCK provided by the external SPI Master in Slave Mode, it is not affected by the setting of the value of the SPIBRR register. However, the maximum speed that can be operated in Slave Mode is affected by the System Clock.

$$SCK\ Baud\ Rate = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$$

or

$$SPIBR = \frac{f_{PCLK}}{2 \times SCK\ Baud\ Rate} - 1$$

13.7 Open-Drain Output for Wired-OR

The SPI bus output does not need to support Open-Drain unless it is a Multiple SPI Master. If an open-drain output is required, the WOMP bit in the SPICTRL register can be set to provide an open-drain output. If set to Open-Drain, a pull-up resistor must be placed on each output line.

13.8 Transfer Size and Direction

The SPISIZE bit in the SPICTRL register selects the transmit size 8/16/32 bits. The MSBF bit in the SPICTRL register allows the start of data transmission to start from MSB (MSBF = 1) or LSB.

13.9 Write Collision

Attempting to write to the SPIDATA register while a transfer is in progress causes a write conflict.

13.10 MODE Fault

When the SPI system is set to Master and the nSS signal input line is asserted, a mode fault error occurs and the MODF bit of SPISTAT is set. Only the master device can generate MODF, which occurs when another SPI device is trying to become a master.

13.11 Interrupt

SPIF Interrupt

This occurs when both the data stored in the FIFO and the TX Shift register are emptied, indicating that the SPI transfer is complete. It is an interrupt that can confirm that the SPI transfer is completed.

MODF Interrupt

Occurs when a Mode fault occurs. A mode fault is a case where two or more masters transmit data when there are multiple masters.

nSS Interrupt

Occurs when a change occurs by sensing the nSS port signal.

TX_FIFO_FULL, TX_FIFO_EMPTY, RX_FIFO_FULL, RX_FIFO_EMPTY

- TX_FIFO_FULL: Indicates that the 8-byte internal FIFO is full. If the TX FIFO is filled with more data in this state, erroneous data transmission is performed.
- TX_FIFO_EMPTY: means that all the data that has been filled in the TX FIFO has been transferred. However, the SPI transmission is not complete because the TX Shift register is not yet emptied.
- RX_FIFO_FULL: Indicates that RX_FIFO is all filled.
- RX_FIFO_EMPTY: means that RX_FIFO is all empty.

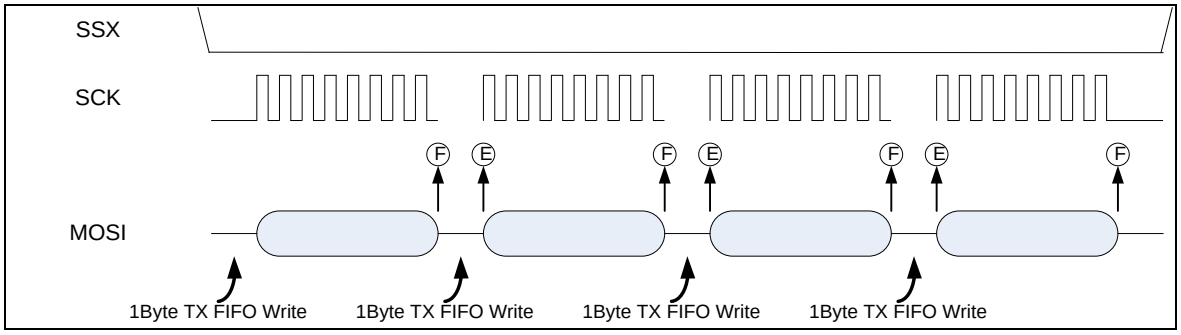


Figure 13-5 1-Byte Transfer vs. Status and Interrupt

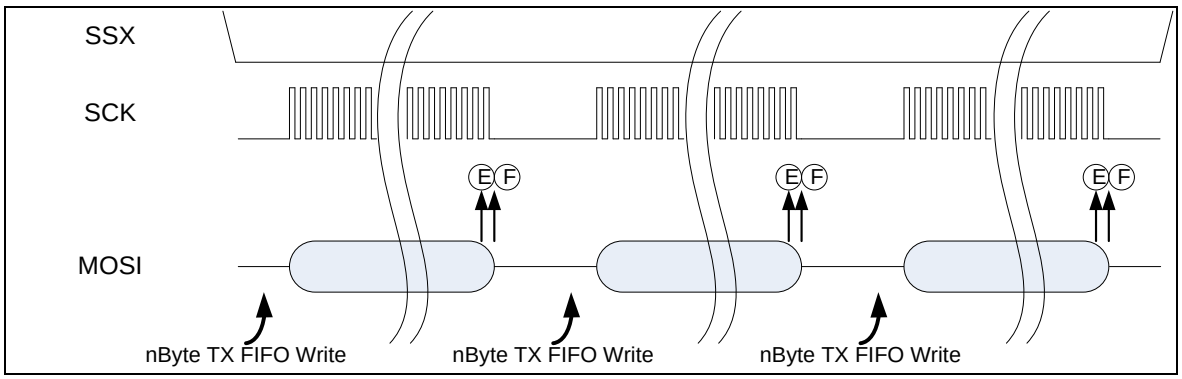


Figure 13-6 n-Bytes Transfer vs. Status and Interrupt

13.12 SPI Control Registers

SPI Control Register (SPICTRL)

Address : 0x8002_1000

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	SPIEN : SPI Enable 0 : SPI is disabled. 1 : SPI is enabled	0
6	R/W	WOMP : Wired-OR Mode for SPI Pins 0 : Outputs have normal CMOS drivers. 1 : Open-drain drivers	0
5	R/W	MSTR : Master/Slave Mode Select 0 : Slave operation 1 : Master operation	0
4	R/W	CPOL : Clock Polarity 0 : The inactive state value of SCK is logic level zero 1 : The inactive state value of SCK is logic level one.	0
3	R/W	CPHA : Clock Phase 0 : Data captured on the leading edge of SCK and changed on the trailing edge of SCK. 1 : Data is changed on the leading edge of SCK and captured on the trailing edge of SCK.	0
2	R/W	MSBF : Most Significant Bit First 0 : Serial data transfer starts with LSB. 1 : Serial data transfer starts with MSB.	0
1 : 0	R/W	SPISIZE : Transfer Data Size 00 : 8-bit data transfer. 01 : 16-bit data transfer. 10 : 32-bit data transfer.	0

SPI Baud Rate Register (SPIBR)

Address : 0x8002_1004

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	R/W	Serial Clock Baud Rate $SCK = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$ Master Mode SCK ≤ System Clock / 2 Slave Mode SCK ≤ System Clock / 4	0xFF

SPI Status Register (SPISTAT)

Address : 0x8002_1008

Bit	R/W	Description	Default Value
15 : 8	R	Reserved	-
7	R	SPIF : SPI Finished Flag 0 : SPI is not finished. 1 : SPI is finished.	0
6	R	WCOL : Write Collision 0 : No attempt to write to the SPDR happened during the serial transfer. 1 : Write collision occurred.	0
5	R	MODF : Mode Fault Flag 0 : Normal operation 1 : Another SPI node requested to become the network SPI master while the SPI was enabled in master mode	0
4	R	nSS : Slave Select Flag 0 : Current Value of nSS port is low 1 : Current Value of nSS port is high	0
3	R	STXF : TX FIFO Full Status bit 0 : FIFO_TX is not full 1 : FIFO_TX is full	0
2	R	STXE : TX FIFO Empty Status bit 0 : FIFO_TX is not empty 1 : FIFO_TX is empty	0
1	R	SRXF : RX FIFO Full Status bit 0 : FIFO_RX is not full 1 : FIFO_RX is full	0
0	R	SRXE : RX FIFO Empty Status bit 0 : FIFO_RX is not empty 1 : FIFO_RX is empty	0

SPI Data Register (SPIDATA)

Address : 0x8002_100C

Bit	R/W	Description	Default Value
31 :0	R/W	SPI Data At 32-bit transfer mode - MSB of Data is SPDR[31] At 16-bit transfer mode - MSB of Data is SPDR[15] At 8-bit transfer mode - MSB of Data is SPDR[7] LSB of Data (received or transmit) is SPDR[0] in any transfer mode	0x0000_0000

SPI nSS Control Register (nSSCTRL)

Address : 0x8002_1010

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	RW	nSSCON : nSS Output Level	1

SPI Interrupt Mask Register (SPIINT)

Address : 0x8002_1014

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	RW	SPIFE : SPIF Interrupt en/disable SPIF Interrupt occurs when transfer has completed. 0 : SPIF interrupt is disabled 1 : SPIF is enabled	0
6	RW	MODFE : MODFI Interrupt en/disable MODFI Interrupt occurs when two more master use data line. 0 : MODFI interrupt is disabled 1 : MODFI is enabled	0
5	R	Reserved	0
4	RW	nSSEN : nSS Interrupt en/disable nSS Interrupt occurs when nSS signal has changed. 0 : nSS Interrupt is disabled 1 : nSS Interrupt is enabled	0
3	RW	STXFE : FIFO_TX_FULL Interrupt en/disable FIFO_TX_FULL Interrupt occurs when FIFO_TX is full 0 : FIFO_TX_FULL Interrupt is disabled 1 : FIFO_TX_FULL Interrupt is enabled	0
2	RW	STXEE : FIFO_TX_EMPTY Interrupt en/disable FIFO_TX_EMPTY Interrupt occurs when FIFO_TX is empty 0 : FIFO_TX_EMPTY Interrupt is disabled 1 : FIFO_TX_EMPTY Interrupt is enabled	0
1	RW	SRXFE : FIFO_RX_FULL Interrupt en/disable FIFO_RX_FULL Interrupt occurs when FIFO_RX is full 0 : FIFO_RX_FULL Interrupt is disabled 1 : FIFO_RX_FULL Interrupt is enabled	0
0	RW	SRXEE : FIFO_RX_EMPTY Interrupt en/disable FIFO_RX_EMPTY Interrupt occurs when FIFO_RX is empty 0 : FIFO_RX_EMPTY Interrupt is disabled 1 : FIFO_RX_EMPTY Interrupt is enabled	0

14 TWI (TWO WIRED INTERFACE)

It has a built-in TWI controller for interfacing with the universal TWI bus. TWI has SCL and SDA signals.

Key Features

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode
- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Multi master operation

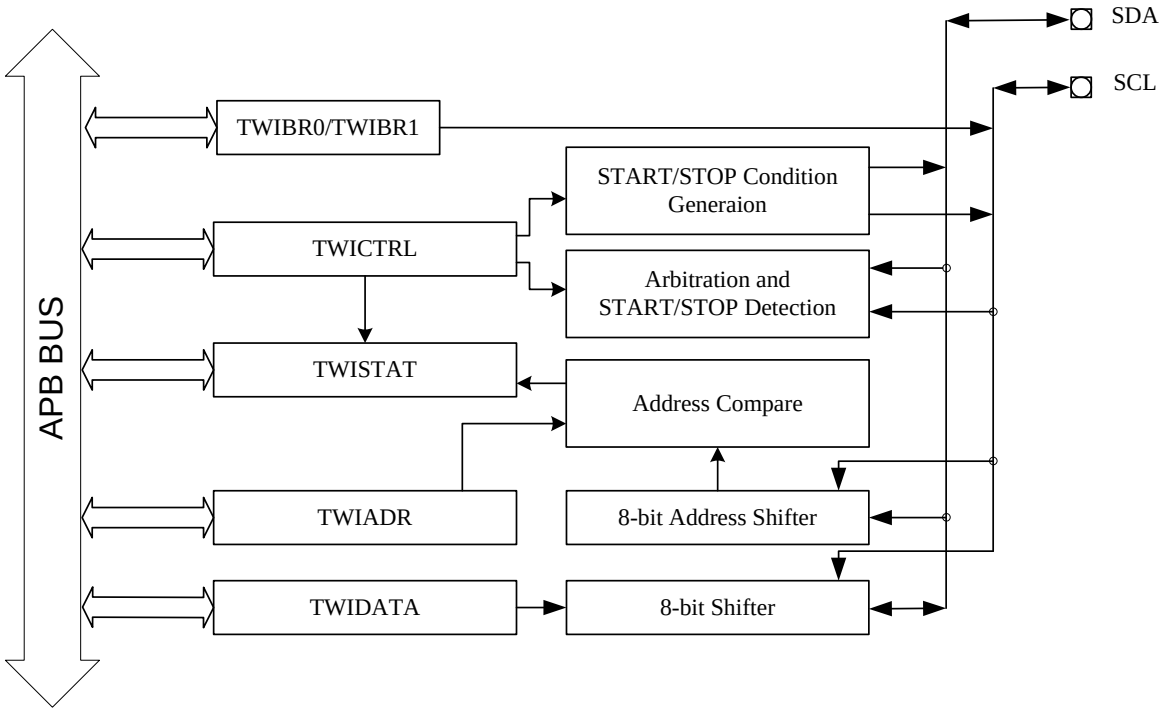


Figure 14-1 TWI Block Diagram

14.1 DATA TRANSFER FORMAT

All data lengths on the SDA line are 8 bits. The number of bytes that can be transmitted per transmission is not limited. The first byte after the start condition is the address field. When the TWI-bus operates in Master mode, the address field is transmitted by the Master. Every byte is followed by an ACK bit. Transmission always starts from the MSB bit of the data and address.

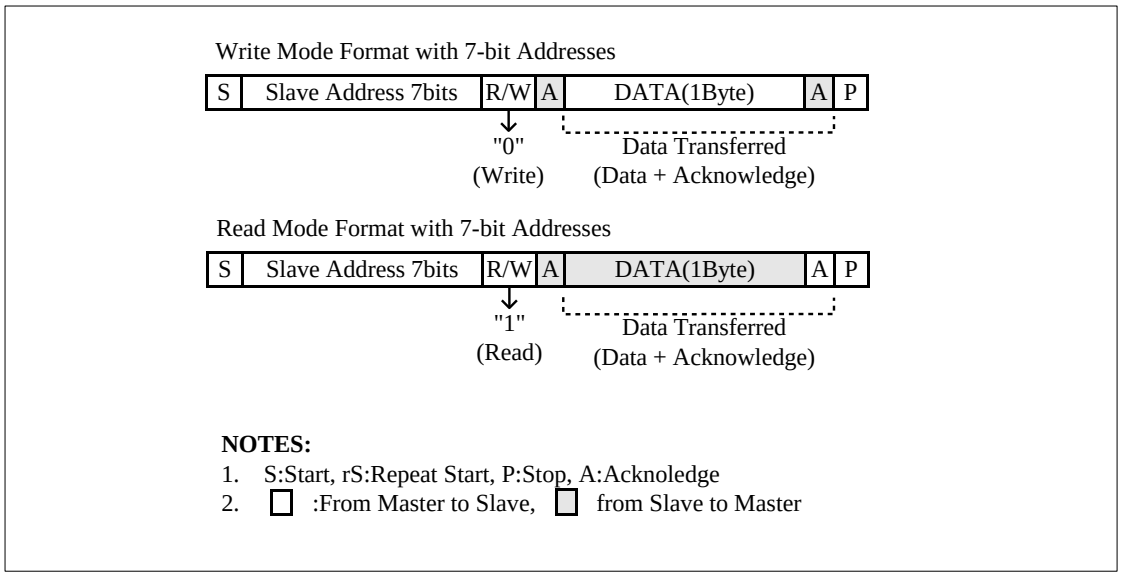


Figure 14-2 TWI-Bus Interface Data Format

14.2 START AND STOP CONDITION

The start condition can transmit 1 byte of data. The stop condition terminates the data transmission. The start condition transitions the SDA line to high-to-low when SCL is high. The stop condition is that the SDA line transitions to low-to-high when SCL is high. When a start condition occurs, the TWI bus becomes busy. After a stop condition occurs, the TWI bus becomes free.

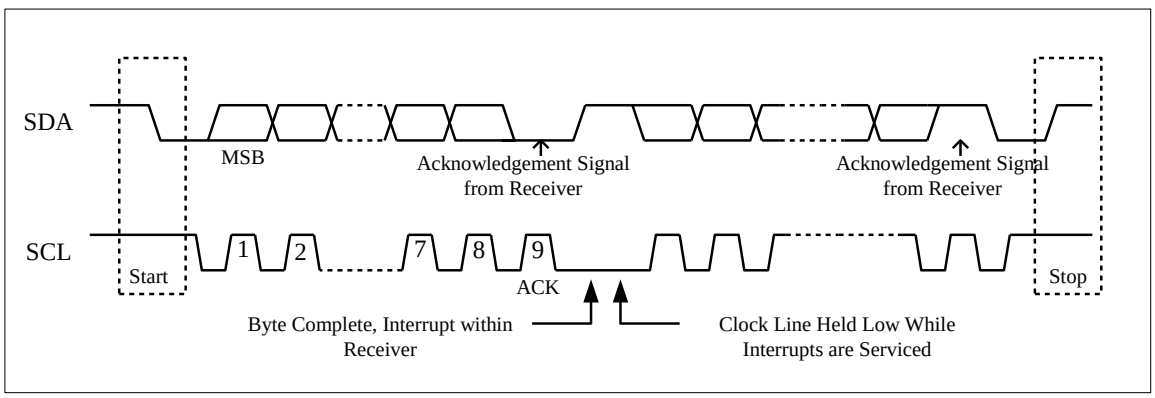


Figure 14-3 Data Transfer on the TWI-Bus

14.3 ACK SIGNAL TRANSMISSION

To completely terminate a byte transmission, the receiving end must send an ACK bit to the transmitting end. The ACK pulse must occur at the ninth clock of the SCL line. Therefore, all nine clocks are needed to transfer one byte of data. Master must generate a clock pulse for ACK bit transmission.

The transmitter must release the SDA line to make the SDA line high when receiving ACK clock pulses. The receiver also keeps the SDA line low when ACK pulses to make SDA "Low" at the ninth "high" interval of SCL.

The ACK bit can be set to either ACK or NOACK by setting the TXACK bit in the control register as a software.

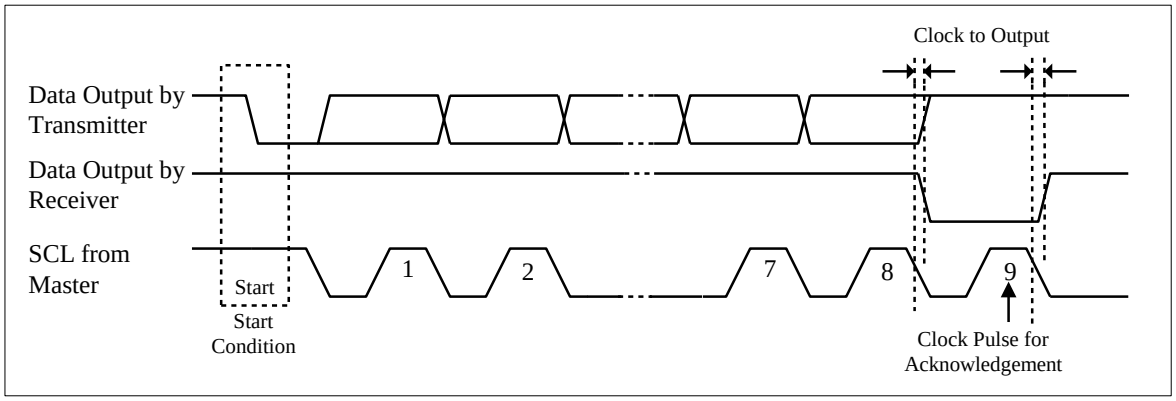


Figure 14-4 Acknowledgement of TWI

14.4 READ-WRITE OPERATION

After transmitting data in the transmit operation mode, the TWI-bus interface must wait until data is ready in the data shifter register. The SCL line will remain low until data is written. SCL is released after new data is written to the data shifter register.

If an interrupt is used, the TWI requests an interrupt after the current data transfer. The CPU writes new data to the buffer after receiving the interrupt request.

After receiving data in receive mode, the TWI bus waits until it reads data. SCL remains LOW until the received data is read. After the new data is read, the SCL is released.

When an interrupt is used, the TWI generates an interrupt after receiving the data, and the CPU receiving the interrupt request reads the data.

14.5 BUS ARBITRATION PROCEDURES

Prevents multiple masters from simultaneously controlling the bus. When a master that has sent a high level to the SDA line recognizes a low level SDA line that another master has sent, it recognizes that the current TWI bus is controlled by a master other than itself, and prevents the data transfer from proceeding any further.

When Device1 and Device2 are operating in master mode at the same time, the appearance of the clock generated on the SCL line is as follows.

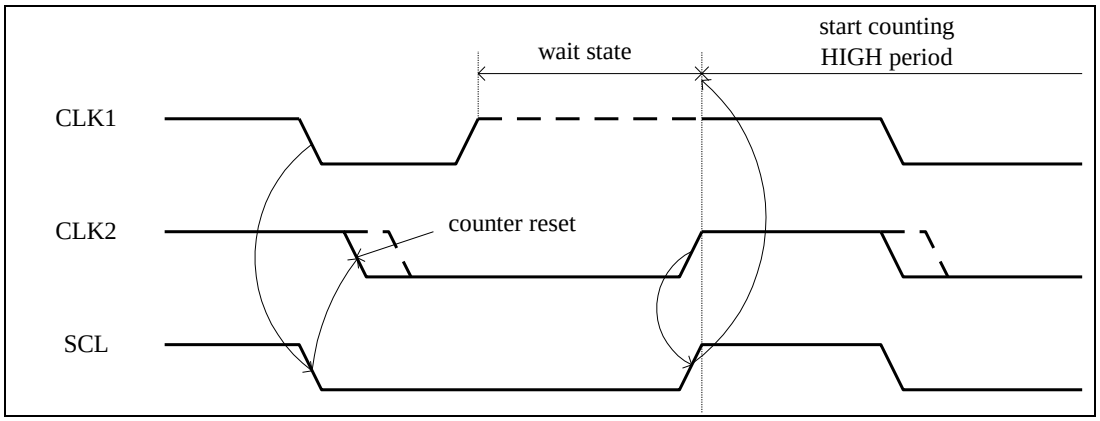


Figure 14-5 Bus arbitration 1 of TWI

In the above situation, according to the data value appearing on the SDA line, the process in which one of Device1 and Device2 takes priority is as follows.

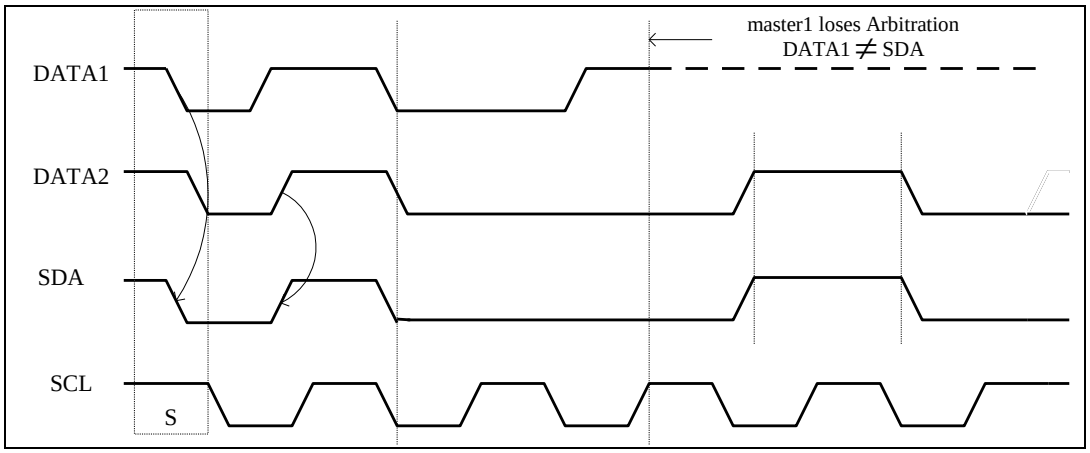


Figure 14-6 Bus arbitration 2

14.6 ABORT CONDITIONS

If no arbitration occurs

1. If the MSTR bit in the TWICTRL register is cleared, a stop condition occurs.
2. No ACK occurs and stop condition occurs. That is, if the SDA signal is not & quot; Low & quot; in the ACK interval.

Arbitration occurs

If the control is lost due to the occurrence of arbitration, the MSTR bit is cleared, but the stop condition does not occur. The currently active SCL clock goes to the end of one byte transmission and SDA, the data output, goes high.

14.7 Operational Flow Diagrams

TWI initialization

TWI must be initialized first.

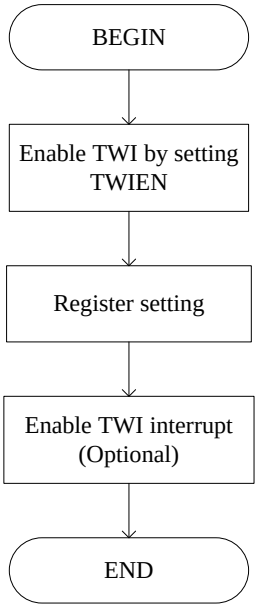


Figure 14-7 TWI Initialization Flow Char

Master Transmit /Receive

Flow chart for data transmission and data reception of TWI. The greatest difference between transmission and reception is that there is a further step of setting the ACK bit to NOACK before receiving the last data at the time of reception. This is to inform the master that the slave is the last received data. In addition, a dummy read stage of the TWIDATA register is required to generate the SCL clock for receiving the actual data

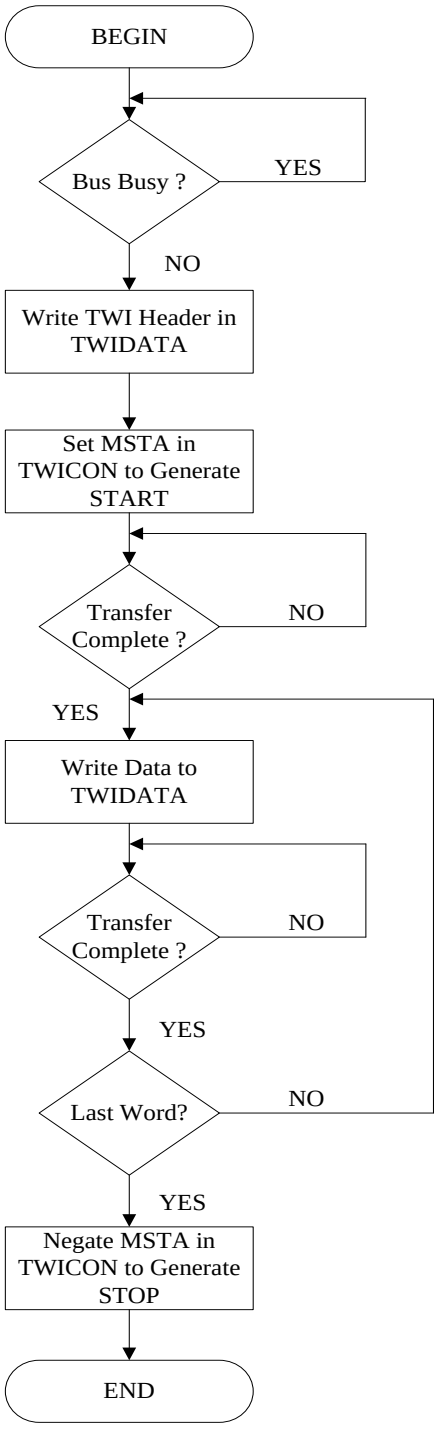


Figure 14-8 Master Transmit Flow Char

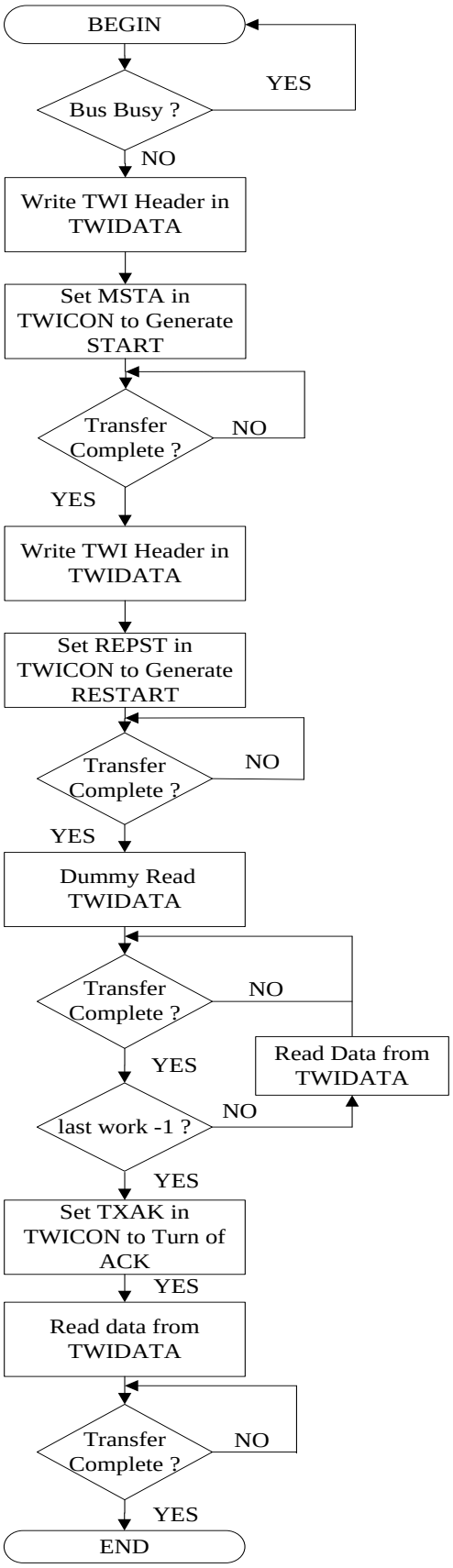


Figure 14-9 Master Receive Flow Char

Slave Mode (Polling mode)

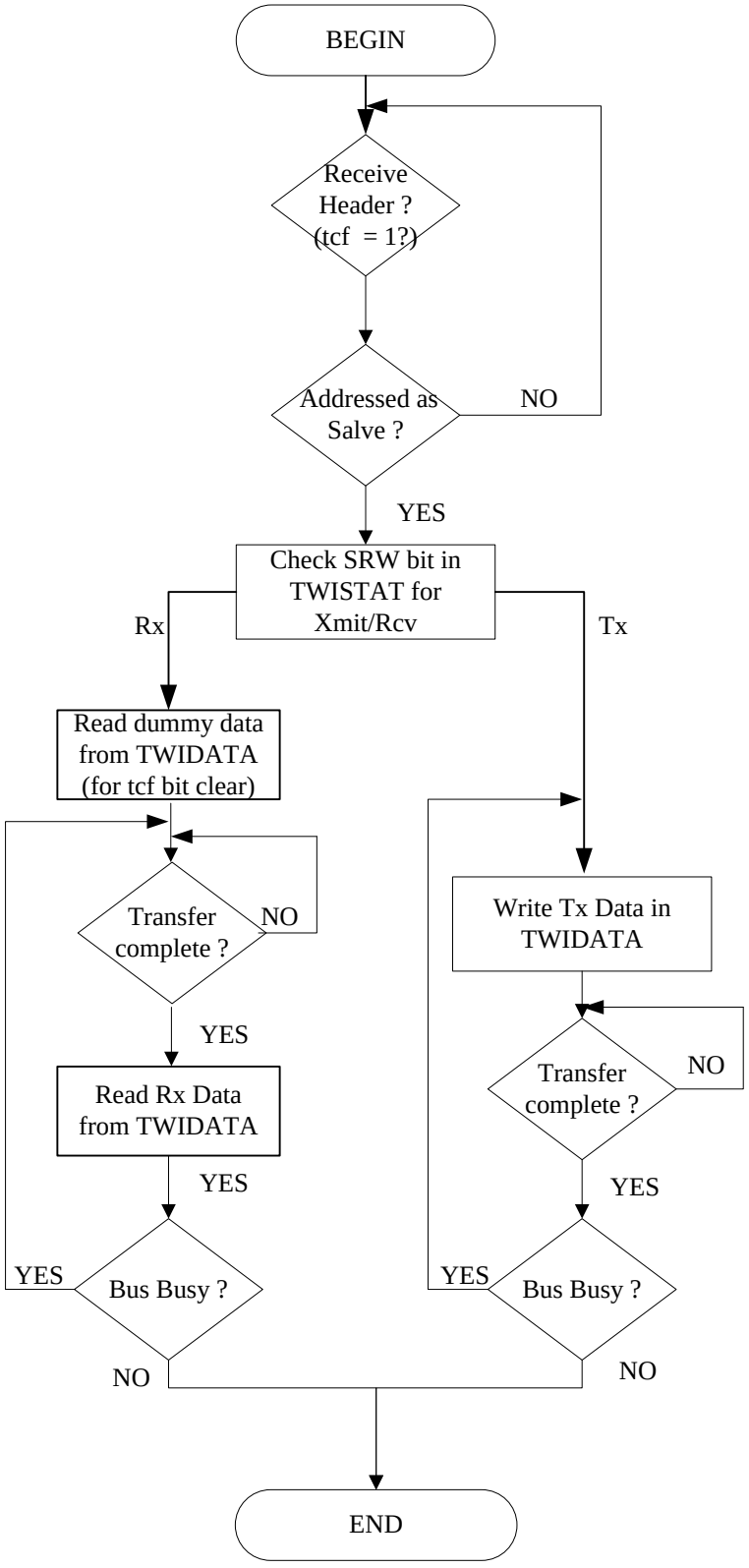


Figure 14-10 Slave Mode Flow Chart (Polling)

Slave Mode (Interrupt mode)

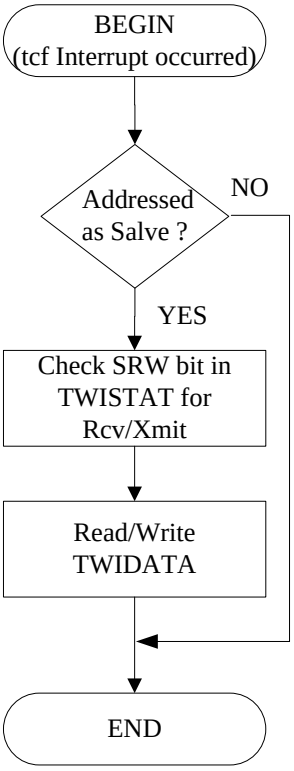


Figure 14-11 Slave Mode Flow Chart (Interrupt)

14.8 TWI Control Registers

TWI Control Register (TWICTRL)

Address : 0x8002_1400

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	–
7	RW	TWIEN : TWI Controller Enable. This bit is set before another register setting for TWI transmission / reception. 0: Disable 1: Enable	0
6	R	Reserved.	–
5	RW	TWIMOD : Master/Slave Mode Select. When changing from 0 to 1, a START condition occurs when Master mode is selected. If clear, a STOP condition occurs and switch to Slave mode. If cleared, even if cleared, the STOP condition does not occur. 0: Generate a STOP condition. 1: Generate START condition.	0
4	RW	TWITR : Transmit/Receive Mode Select. Determine the transfer operation in Master Mode. 0: TWI Master reception 1: TWI Master transmission	0
3	RW	TWIAK : Transmit Acknowledge Enable. This bit determines the value of the SDA line during the ACK interval. In Master Receive Mode, when the last byte is transmitted, NO ACK indicates that the data transmission is last. If NO ACK after the last transmission, a STOP condition is generated. 0: ACK bit = & quot; 0 & quot; - ACK (acknowledge) 1: ACK bit = "1" - NO ACK (no acknowledge)	0
2	RW	REPST : Repeated Start. When this bit is set to 1, the TWI controller generates a Repeated START condition when it is Master. It is cleared when Repeated START condition occurs. 0: N / A 1: Generate Repeated START condition.	0
1	R/W	TCIE : Transfer complete Interrupt enable bit When data transfer of 1-byte unit is completed, it is determined whether or not an interrupt is generated. 0: Disable 1: Enable	0
0	R/W	LSTIE : Lost arbitration Interrupt enable bit When operating as a master, if transfer permission is lost, it is determined whether an interrupt is generated. 0: Disable 1: Enable	0

TWI Status Register (TWISTAT)

Address : 0x8002_1404

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9	RW	TXEMPTY : TX Buffer Empty. Indicates the status of the transmit buffer. When it is 0, the desired value can be written. 0: There is data to be sent to the transmit buffer 1: Transmit buffer is empty	1
8	RW	RXFULL : RX Buffer Full. Indicates the status of the receive buffer. When it is 1, the desired value can be written. 0: Receive buffer is empty 1: Receive buffer has data to read	0
7	R	TWIDT : Data Transferring Bit. It is set each time a byte is transmitted, and is cleared when reading or writing the TWIDATA register. When 1 is written to this bit, it is cleared. 0: Transferring bytes 1: One byte transfer complete	0
6	R	TWIAS : Addressed as Slave Bit. The TWI controller acts as a slave when its address matches the address received. The TWICON register is written or cleared when a STOP condition occurs. 0: Address does not match 1: Address matches	0
5	R	TWIBUSY : Bus Busy Bit. Indicates the TWI bus state. It is set by the START condition and cleared by the STOP condition. A write of 0 to this bit is also cleared. 0: Bus idle state 1: Bus busy status	0
4	RW	TWILOST : Lost Arbitration Bit. When the TWI controller is in master mode, it is set if the control of the bus is lost. It should be cleared by software. When 1 is written, it is cleared. 0: Lost arbitration did not occur. 1: Lost arbitration occurred.	0
3	R	TWISRW : Slave Read/Write Bit. Indicates sending / receiving operation when TWI controller is in slave mode. 0: Slave reception mode 1: Slave transmission mode	0
2	R	Reserved.	-
1	RW	RSF : Repeated start flag Repeated A flag bit to check if a START condition	0

		has occurred. It is set when a Repeated START condition occurs and is cleared when a STOP condition occurs or a 1 is written to this bit when set. 0: Repeated START condition did not occur or STOP condition occurred. 1: Repeated START condition occurred.	
0	R	TWIRXAK : Received Acknowledge Bit. Means the value of the SDA line in the ACK interval. 0: Receive acknowledge 1: No Acknowledge reception	1

TWI Address Register(TWIADR)

Address : 0x8002_1408

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7: 0	RW	(At only slave mode) 7-bit slave address. Represents the TWI controller's device address. [7:1] = Slave Address [0] = Not mapped	0x00

TWI Data Register (TWIDATA)

Address : 0x8002_140C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	RW	TWI data: Represents TWI data. Write - the address of the data to be transmitted or the device to be accessed. Read - Received data	0x00

TWI Baud-Rate 0 Register (TWIBR0)

Address : 0x8002_1410

Bit	R/W	Description	Default Value
31 : 4	R	Reserved.	-
7 : 0	RW	Baud-rate 0 Value. TWIBR0 ≥ 3	0x0F

TWI Baud-Rate 1 Register (TWIBR1)

Address : 0x8002_1414

Bit	R/W	Description	Default Value
31 : 9	R	Reserved.	-
8 : 0	RW	Baud-rate 1 Value.. TWIBR1 ≥ 0	0xFF

$$TWIBR0 = f_{PCLK} \times 700ns + 3$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)}$$

$$TWIBR1 = \frac{f_{PCLK}}{2SCL} - \frac{TWIBR0 + 7}{2}$$

* f_{PCLK} = AMBA APB clock frequency

* SCL = TWI transmission rate

ex) When the APB clock is 50MHz and the TWI transfer rate is 400Kbps, (f_{PCLK} = 50MHz, SCL = 400Kbps)

$$TWIBR0 = 50MHz \times 700ns + 3 = 50 \times 10^6 \times 700 \times 10^{-9} + 3 = 38$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)} \Rightarrow 400Kbps = \frac{50MHz}{(2TWIBR1 + 38 + 7)} \Rightarrow 400 \times 10^3 = \frac{50 \times 10^6}{(2TWIBR1 + 45)}$$

<Baud-rate Register Setting Reference Table>

f_{PCLK}	TWIBR0	TWIBR1			
		400Kbps	300Kbps	200Kbps	100Kbps
48Mhz	37(0x25)	38(0x26)	58(0x3A)	98(0x62)	218(0xDA)
24Mhz	20(0x14)	17(0x11)	27(0x1B)	47(0x2F)	107(0x6B)
12Mhz	12(0xC)	6(0x6)	11(0xB)	21(0x15)	51(0x33)
6Mhz	7(0x7)	1(0x0)	3(0x3)	8(0x8)	23(0x17)
11.2896Mhz	11(0xB)	5(0x5)	10(0xA)	19(0x13)	48(0x30)
5.6448Mhz	7(0x7)	0(0x0)	3(0x3)	7(0x8)	21(0x16)

* The values in the table above may have some errors.

15 KEYSCAN

The Key Scan Controller can control up to 2x2 Key Matrix. Scan cycle setting is supported.

Key Features

- Scan Mode. (Key press, Key press / release) support
- Scan Period support
- Binary format and hexadecimal format support

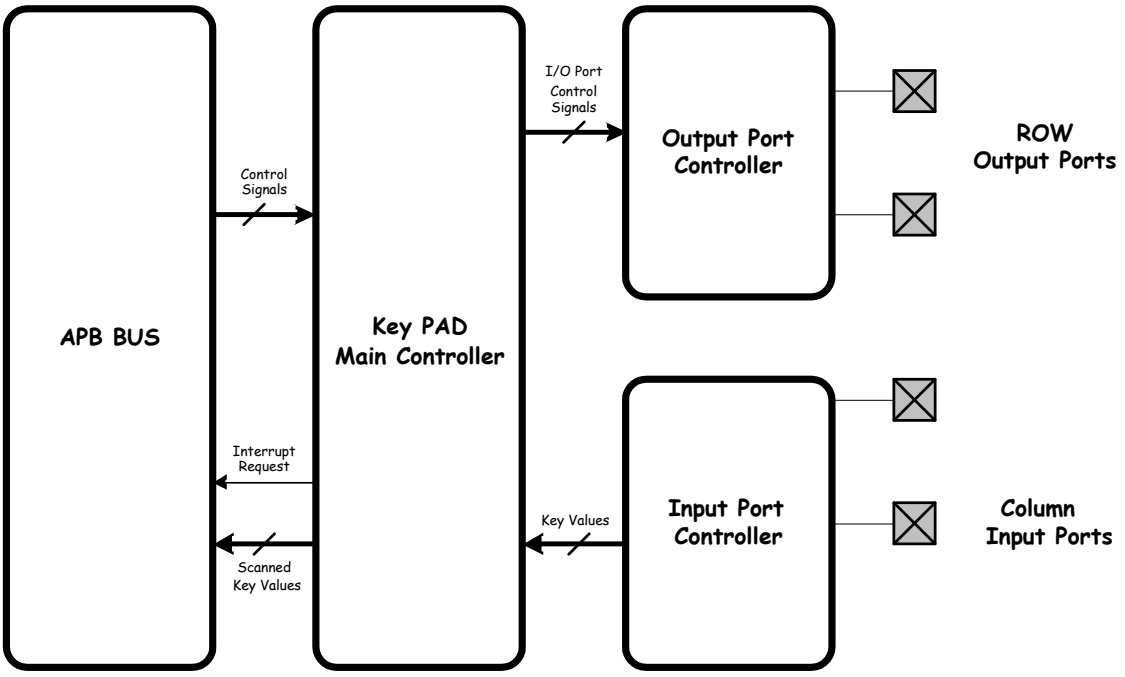


Figure 15-1 Key Scan Block Diagram

15.1 Key Scan Matrix Circuit

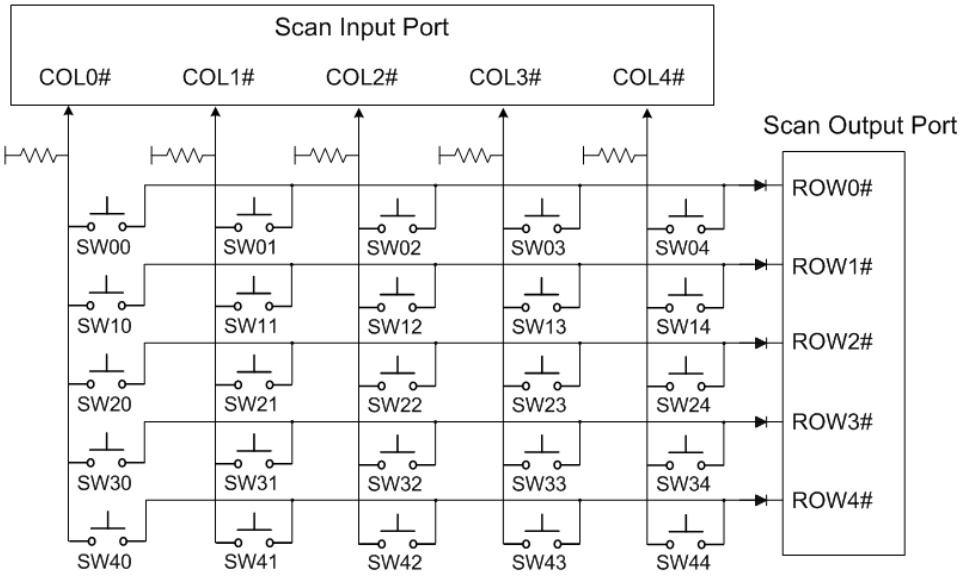


Figure 15-2 5 x 5 Key Matrix

When SW is pressed, the corresponding bit is set to "1" to generate an interrupt. When configuring the key scan circuit, it is a diode connected to the scan output port (ROWx pin). If there is no diode, the key value will not be recognized when you press more than one switch in the same column.

15.2 Key Scan mode and Interrupt

In Key Press Mode, the KSD1 and KSD2 register values are changed while interrupts occur only when the switch is pressed.

In Key Press / Release Mode, KSD1 and KSD2 register values are changed while interrupts occur both when the switch is pressed and released.

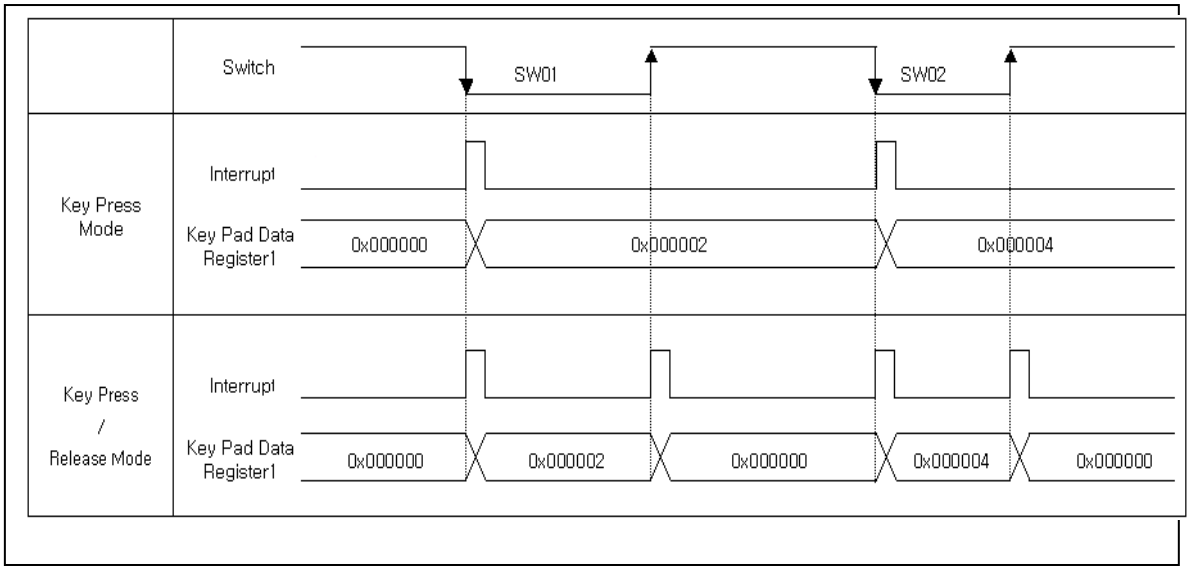


Figure 15-3 Key Scan Time Diagram

15.3 Key Scan Control Registers

Key Scan Control Register (KSCTRL)

Address : 0x8002_1800

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	-
2	R/W	Key Scan Mode Select bits 0 : Key press mode 1 : Key press / release mode	0
1	R	Reserved	-
0	R/W	Key Scan Enable bit 0: Scan Disable 1: Scan Enable	0

Key Scan Counter Register (KSCNT)

Address : 0x8002_1804

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	Scan clock divide ratio setting bits.	0xFFFF

$$Scanning \quad Frequency = \frac{f_{PCLK}}{11 \times (KSCNT + 1)}$$

Key Scan Data 1 Register (KSD1)

Address: 0x8002_1808

Bit	R/W	Description	Default Value
31 : 17	R	Reserved	-
16	R	Reserved	0
15	R	Reserved	0
14	R	Reserved	0
13	R	Reserved	0
12	R	Reserved	0
11	R	Reserved	0
10	R	Reserved	0
9	R	Reserved	0
8	R	Reserved	0
7	R	Reserved	0
6	R	SW11	0
5	R	SW10	0
4	R	Reserved	0
3	R	Reserved	0
2	R	Reserved	0
1	R	SW01	0
0	R	SW00	0

Key Scan Data 2 Register (KSD2)

Address: 8002 180Ch

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
4: 0	R	Scanned Switch value (Represented as hexadecimal Value)	0x00

*** Key Scan Data 1 Represents the value of the register in hexadecimal. (SW03 is represented by 0x04)

*** (Note) If two or more keys are pressed, the value of this register is set to "0x0".

16 REAL TIMER CLOCK

The RTC operates using a clock of 32.768 kHz and can set the year, month, day, hour, minute, and second registers and read the current time. It also causes periodic interrupts.

Key Features

- Power independence
- Leap year support
- periodic interrupt generation

16.1 RTC Control Registers

Real Time Counter Control Register (RTCCTRL)

Address : 0x8002_1C00

Bit	R/W	Description	Default Value
31 : 25	R	Reserved	-
24	R	Register update bit 0 : Update 1 : Not Yet Update The update bit must be set before the RTC setting is passed.	0
23 : 8	R	Reserved	-
8	R/W	Test mode	0
7 : 4	R/W	Interrupt select 0000 : Timer 0001 : Alarm 0010 : 0.25 Sec 0011 : 0.5 Sec 0100 : 1 Sec 0101 : 2 Sec 0110 : 4 Sec 0111 : Reserved 1000 : 1 Min 1001 : 2 Min 1010 : 4 Min 1011 : Reserved 1100 : 1 Hour 1101 : 2 Hour 1110 : 4 Hour 1111 : 1 Day	0000
3	R/W	Interrupt enable bit 0 : Disable 1 : Enable	0
2	R/W	Temperature compensation enable bit 0 : Disable 1 : Enable	0
1	R/W	Timer counter enable bit 0 : Disable 1 : Enable	0
0	R/W	1Hz counter enable bit 0 : Disable 1 : Enable	0

*** After setting the RTCCTRL register, check the register update bit in the RTCCTRL register.

Real Time Counter Initialization Register (RTCINIT)

Address : 0x8002_1C04

Bit	R/W	Description	Default Value
31 : 15	R	Reserved	-
14 : 0	R/W	1Hz counter	0

*** After setting the RTCINIT register, check the register update bit in the RTCCTRL register.

Real Time Counter Clock Register (RTCCLK)

Address : 0x8002_1C08

Bit	R/W	Description	Default Value
31 : 21	R	Reserved	-
20 : 16	R/W	Hour (0~23)	0
15 : 14	R	Reserved	-
13 : 8	R/W	Min (0~59)	0
7 : 6	R	Reserved	-
5 : 0	R/W	Sec (0~59)	0

*** After setting the RTCCLK register, check the Register update bit in the RTCCTRL register.

Real Time Counter Calendar Register (RTCCLD)

Address : 0x8002_1C0C

Bit	R/W	Description	Default Value
31 : 23	R	Reserved	-
22 : 16	R/W	Year (0~99)	0x04
15 : 12	R/W	Month (0~11)	0x0
11	R	Reserved	-
10 : 8	R/W	Week (0~6)	0x4
7 : 5	R	Reserved	-
4 : 0	R/W	Day (1~31)	0x01

*** After setting the RTCCLD register, check the register update bit in the RTCCTRL register.

Real Time Counter Timer Register (RTCTIMER)

Address : 0x8002_1C10

Bit	R/W	Description	Default Value
31 : 0	R/W	RTC timer counter 32-bit value. Down counter	0xFFFF_FFFF

*** After setting the RTCTIMER register, check the register update bit in the RTCCTRL register.

*** The down counter value of the RTCTIMER register is set by subtracting 1 from the desired cycle.

*** The down counter value of the RTCTIMER register is prohibited to be set below 0x7.

Real Time Counter Alarm Register (RTCALM)

Address : 0x8002_1C14

Bit	R/W	Description	Default Value
31 : 24	R	Reserved	-
23 : 21	R	Reserved	-
20 : 16	R/W	Hour(0~23)	0x00
15 : 14	R	Reserved	-
13 : 8	R/W	Min(0~59)	0x00
7 : 6	R	Reserved	-
5 : 0	R/W	Sec(0~59)	0x00

*** After setting the RTCALM register, check the register update bit in the RTCCTRL

register.

Temperature Compensation Threshold Register (TEMPTHR)

Address : 0x8002_1C20

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R/W	Threshold temperature changes to generate interrupt	0

*** After setting the TEMPTHR register, check the register update bit in the RTCCTRL register.

Temperature Compensation PPM ADJ Register (TEMPPPMADJ)

Address : 0x8002_1C24

Bit	R/W	Description	Default Value
31 : 0	R/W	PPM ADJ	0

*** After setting the TEMPPPMADJ register, check the register update bit in the RTCCTRL register.

Temperature Compensation PPM OSC Register (TEMPPPMOSC)

Address : 0x8002_1C28

Bit	R/W	Description	Default Value
31 : 26	R/W	Reserved	0
25 : 0	R	PPM OSC	0

*** After setting the TEMPPPMOSC register, check the register update bit in the RTCCTRL register.

Temperature Compensation OSC CAP Register (TEMPOSCCAP)

Address : 0x8002_1C2C

Bit	R/W	Description	Default Value
31 : 7	R/W	Reserved	0
6 : 0	R/W	Oscillator Capacitance	0

*** After setting the TEMPOSCCAP register, you must check the register update bit in the RTCCTRL register.

17 EMB RESISTERS

The EMB (Energy Measurement Block) functions to calculate the power consumption by receiving the voltage and current signals sampled by the ADC. EMB registers are divided into three types: calibration register, EMB input register, and EMB output register.

Key Feature

- Fast Calibration
- Fully Hardwired Energy measurement

17.1 EMB Operation Control Register (EMB_OP)

Address: 0x8002_2000

Bit	*R/W*	*Description*	*Default Value*
31:18	R	Reserved	1010000b
17:15	R/W	ADC resolution 0 : 17bit 1 : 18bit 2 : 19bit 3 : 20bit 4 : 21bit 5 : 22bit	101b
14:11	R/W	Reserved	0000
10	R/W	DFC_CLK_SEL 0 : emb_clk_x8 1 : emb_clk_x32	0
9	R/W	Phase fail detection enable 0 : Disable PFail interrupt 1 : Enable PFail interrupt	0
8	R/W	SAG detection enable 0 : Disable SAG interrupt 1 : Enable SAG interrupt	0
7:6	R/W	Reserved	01b
5	R/W	Phase A enable	0
4	R/W	Phase B enable	0
3:0	R/W	Reserved	0

DFC_CLK_SEL can be used to select the clock input to the DMB (Digital Frequency Counter) block of the EMB.

The SEM8310S chip has dedicated hardware to detect the SAG / Swell detection immediately after SAG or swell occurrence in the EMB and the Power Fail (voltage imaging) which is defined by the user for a certain time. This is explained in chapters 17.6 and 17.7, respectively. EMB_OP [8] is a bit for enabling / disabling SAG / SWELL detection and EMB_OP [9] is a bit for enabling / disabling voltage imaging detection.

17.2 EMB Calibration Register

Address	*Bit*	*Register*	*Description*
0x8002_2014	22	CAL_VGAIN_A	A constant that multiplies the voltage channel, regulates the voltage gain.
0x8002_2018	22	CAL_IGAIN_A	A constant multiplied to the current channel to regulate the current gain.
0x8002_201C	22	CAL_IGAIN_D	
0x8002_2020	22	CAL_PHCAL_A	A constant that compensates for the phase difference between the voltage channel and the current channel, and the channel that is subject to phase correction is determined by the CAL_PHSEL register.
0x8002_2024	22	CAL_PHSEL_A	0: Perform phase compensation for voltage channel 1: Perform phase correction for current channels
0x8002_2028	22	CAL_PGAIN_A	Is a constant that adjusts the gain of the active power.
0x8002_202C	22	CAL_QGAIN_A	Is a constant that regulates the gain of the reactive power.
0x8002_2030	22	CAL_VMG_A	Is a constant that adjusts the gain of the effective voltage.
0x8002_2034	22	CAL_IMG_A	Is a constant that regulates the gain of the effective current.
0x8002_2038	22	CAL_IMG_D	
0x8002_203C	signed, 22	CAL_VDC_A	Constant for voltage channel, removes DC offset.
0x8002_2040	signed, 22	CAL_IDC_A	Constant to current channel, removes DC offset.
0x8002_2044	signed, 22	CAL_IDC_D	

The SEM8310S does not need to perform the calculation or to store the values in the calibration process, since the calibration signal is supplied to the SEM8310S to perform the calibration and the result is stored only by a single calibration command.
The six registers CAL_VDC_A, CAL_IDC_A, CAL_VGAIN_A, CAL_IGAIN_A, CAL_PHSEL_A and CAL_PHCAL_A are the basic registers for the normal operation of the EMB. CAL_PGAIN_A, CAL_QGAIN_A, CAL_VMG_A and CAL_IMG_A are the registers for fine tuning to improve the EMB performance. The application of each calibration register inside the EMB can be seen in Figure 17-2.

17.3 EMB I / O register

The SEM8310S has several configurable registers to accommodate different watt-hour metrics.
The DFC_GAIN register changes according to the meter constant of the watt hour meter, and the PNLTH and QNLTH registers control the start current according to each performance class of the watt hour meter. Finally, the SEM8310S generates several kinds of power quantities at the same time, and the internal multiplexer selects the two power quantities to be output to the outside by the PULSE_OUT_SEL1 and PULSE_OUT_SEL2 registers. The SEM8310S can generate nine different power values and corresponding nine different pulse outputs, with one external power input register and a corresponding

energy accumulator. The register that is the input of the external power accumulator is the EXT_POWER1 register.
Table 17.3-1 provides a brief description of the EMB input registers.

Table 17.3-1 EMB Input Registers

Address	*Bit*	*Register*	*Description*
0x8002_2048	32	DFC_GAIN	Register corresponding to the instrument constant
0x8002_204C	16	DFC_DUTY	Output pulse duration
0x8002_2050	19	PNLTH	A register corresponding to the starting current in PF1
0x8002_2054	19	QNLTH	A register corresponding to the starting current in PF0
0x8002_2084	18	SP_DIFF_TH	A register for adjusting the starting current in PF0
0x8002_2088	1	REACT_SEL	Reactive power accumulation method selection register
0x8002_2090	11	DFC_RUN_SEL	Register to select DFC to operate
0x8002_2094	4	PULSE_OUT_SEL1	LED1 Register to select pulse output
0x8002_2098	4	PULSE_OUT_SEL2	LFD2 Register to select pulse output
0x8002_20CC	32	EXT_POWER1	External input power

The SEM8310S calculates the effective voltage, effective current, active power, reactive power, apparent power, active power, reactive power, and apparent power, and simultaneously detects the transmission / reception state. Each power accumulator accumulates the corresponding amount of power and converts the cumulative amount of power into a corresponding register and output pulse, respectively. Table 17.3-2 shows the EMB output registers..

Table 17.3-2 EMB Output Resisters

Address	*Bit*	*Register*	*Description*
0x8002_20A8	2	FD_A	Transmission / reception state 0: Fault effective power, Transmission faults Reactive power 1: Fault effective power, Fault ground reactive power 2: Transmission active power, Transmission ground reactive power 3: Transmission power active power, power reception phase reactive power
0x8002_20AC	21	VRMS_A	Effective voltage LSB = Vn x V_ratio x 1.192093 x 10-7 V (Vn: rated voltage [V], V_ratio: voltage constant)
0x8002_20B0	21	IRMS_A	Effective current LSB = Imax x I_ratio x 1.192093 x 10-7A (Imax: maximum current [A], I_ratio: current constant)
0x8002_20B4	21	IRMS_D	

0x8002_20C4	signed, 19	WATT_A	Active power LSB = Vn x V_ratio x Imax x I_ratio x 1.192093 x 10^{-7} W
0x8002_20C8	signed, 19	VAR_A	Reactive power LSB = Vn x V_ratio x Imax x I_ratio x 1.192093 x 10^{-7} VAR
0x8002_20C0	18	VA_A	Apparent power LSB = Vn x V_ratio x Imax x I_ratio x 1.192093 x 10^{-7} VA
0x8002_20D4	32	IMPORT_WH	Effective power of faucet LSB = 100 / K Wh (K: Gauge constant[imp/KWh])
0x8002_20D8	32	EXPORT_WH	Effective power transmission capacity LSB = 100 / K Wh
0x8002_20DC	32	VAH	Apparent power LSB = 100 / K VAh
0x8002_20E0	32	IMPORT_VARH	Reactor reactive power LSB = 100 / K VARh
0x8002_20E4	32	EXPORT_VARH	Power transmission reactive power LSB = 100 / K VARh
0x8002_20E8	32	IMPORT_LAG_VARH	Reactor ground reactive power LSB = 100 / K VARh
0x8002_20EC	32	IMPORT_LEAD_VARH	Reactor phase Reactive power LSB = 100 / K VARh
0x8002_20F0	32	EXPORT_LAG_VARH	Transmission ground reactive power LSB = 100 / K VARh
0x8002_20F4	32	EXPORT_LEAD_VARH	Transmission power phase reactive power LSB = 100 / K VARh
0x8002_20F8	32	EXT_ENERGY1	External power 1 LSB = 100 / K Wh

The FD register compares the sign of the active power and the reactive power of each phase to determine the transmission / reception state. The analysis on the quadrant is shown in Figure 17-1.

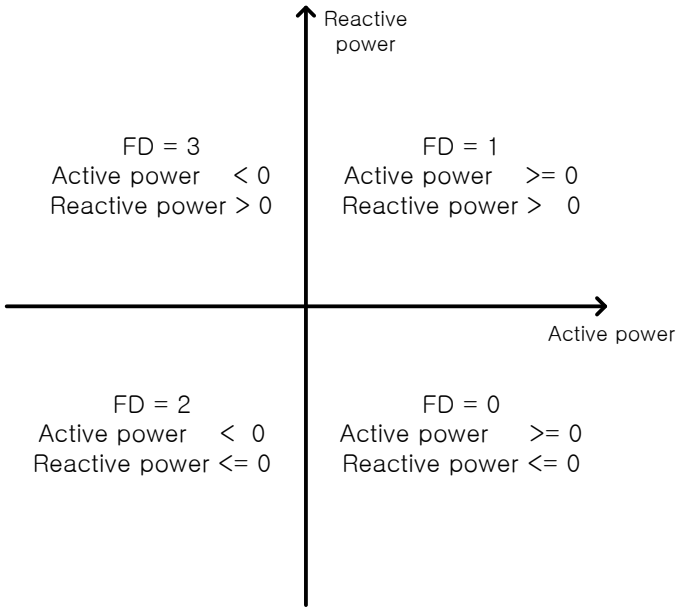


Figure 17-1 Determining the FD Register

Figure 17-2 shows the application of each EMB output register.

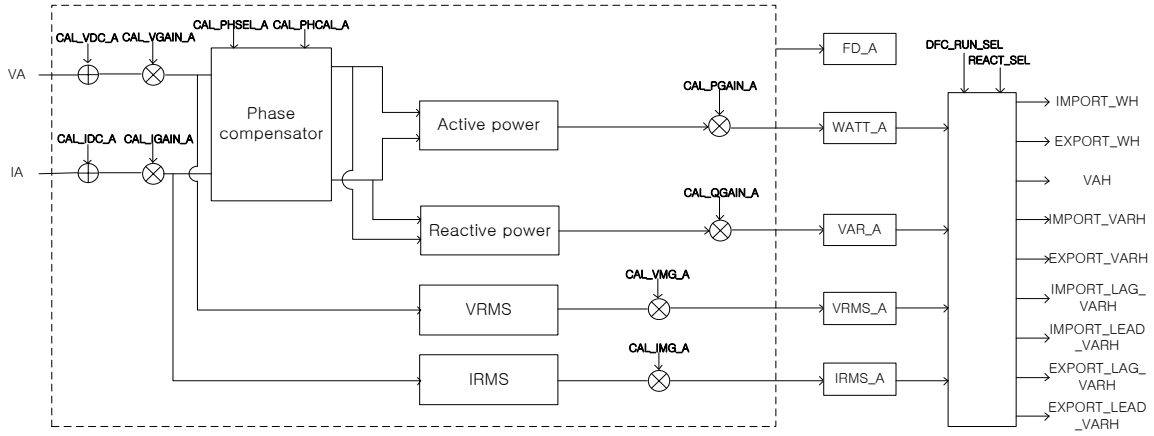


Figure 17-2 EMB Output Registers

17.4 Generation of each energy amount and pulse output

SEM8310S can obtain 10 different energy quantities at the same time by using EMB output values WATT_A, VAR_A, VA_A and so on. Each energy amount is divided into four kinds of active power, apparent power, reactive power, and external input power. The DFC_RUN_SEL register is a register that determines the amount of energy to be accumulated. If DFC_RUN_SEL = 111_1111_x111b, all declared energy amount is accumulated. If DFC_RUN_SEL = 000_0000_x000b, no energy amount is accumulated. Table 17.4-1 shows the detailed settings of the DFC_RUN_SEL register.

Table 17.4-1 DFC_RUN_SEL Register

DFC_RUN_SEL register	Designated energy quantity
DFC_RUN_SEL[10]	IMPORT_WH
DFC_RUN_SEL[9]	EXPORT_WH
DFC_RUN_SEL[8]	VAH
DFC_RUN_SEL[7]	IMPORT_VARH
DFC_RUN_SEL[6]	EXPORT_VARH

DFC_RUN_SEL[5]	IMPORT_LAG_VARH
DFC_RUN_SEL[4]	IMPORT_LEAD_VARH
DFC_RUN_SEL[3]	Not used
DFC_RUN_SEL[2]	EXPORT_LEAD_VARH
DFC_RUN_SEL[1]	EXT_ENERGY1
DFC_RUN_SEL[0]	EXPORT_LAG_VARH

Each power amount is obtained by a combination of WATT_A, VAR_A and VA_A register values. The effective power amount is WATT_A, the reactive power amount is VAR_A, and the apparent power amount is VA_A. The accumulation of power is basically made by using the sum of input power, and the sign of each power register determines the direction of transmission / reception of the amount of power.

Active energy
Since WATT_A can be positive or negative, there are two types of active energy available:.

$$\text{IMPORT\_WH} = \int (WATT\_A)dt, \quad \text{when WATT\_A} \geq 0,$$

$$\text{EXPORT\_WH} = \int (WATT\_A)dt, \quad \text{when WATT\_A} < 0,$$

Apparent power
Since the apparent power VAH is always positive, the apparent power is defined as follows.

$$\text{VAH} = \int (VA\_A)dt$$

Reactive power
Obtaining the reactive power amount is slightly more complicated than obtaining the effective power amount. When REACT_SEL = 0h, the accumulation of each reactive power amount is made according to the sign of the corresponding reactive power, and the accumulation of each reactive power amount when REACT_SEL = 1h is made according to the sign of the corresponding active power. Figure 17-3 and Figure 17-4 show the accumulation method of reactive power amount in each quadrant.

When REACT_SEL = 0:

$$\text{IMPORT\_VARH} = \int (VAR\_A)dt, \quad \text{when VAR\_A} \geq 0,$$

$$\text{EXPORT\_VARH} = \int (VAR\_A)dt, \quad \text{when VAR\_A} < 0,$$

$$\text{IMPORT\_LAG\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} \geq 0 \,\&\, \text{VAR\_A} \geq 0,$$

$$\text{IMPORT\_LEAD\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} < 0 \,\&\, \text{VAR\_A} \geq 0,$$

$$\text{EXPORT\_LAG\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} < 0 \,\&\, \text{VAR\_A} < 0,$$

$$\text{EXPORT\_LEAD\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} \geq 0 \,\&\, \text{VAR\_A} < 0$$

When REACT_SEL = 1 (according to KEPCO purchase specifications):

$$\text{IMPORT\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} \geq 0,$$

$$\text{EXPORT\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} < 0,$$

$$\text{IMPORT\_LAG\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} \geq 0 \,\&\, \text{VAR\_A} \geq 0,$$

$$\text{IMPORT\_LEAD\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} \geq 0 \,\&\, \text{VAR\_A} < 0,$$

$$\text{EXPORT\_LAG\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} < 0 \,\&\, \text{VAR\_A} < 0,$$

$$\text{EXPORT\_LEAD\_VARH} = \int (VAR\_A)dt, \quad \text{when WATT\_A} < 0 \,\&\, \text{VAR\_A} \geq 0$$

External input power amount

EXT_POWER1, the external input power register, is prepared for the case where it is necessary to find the amount of power other than the predefined amount of power in SEM8310S. If necessary, the EXT_POWER1 register can have its value as a combination of WATT_A, VAR_A, and VA_A. When DFC_RUN_SEL [1] = 1, the EXT_ENERGY1 register accumulates the value of the EXT_POWER1 register and calculates the corresponding power amount.

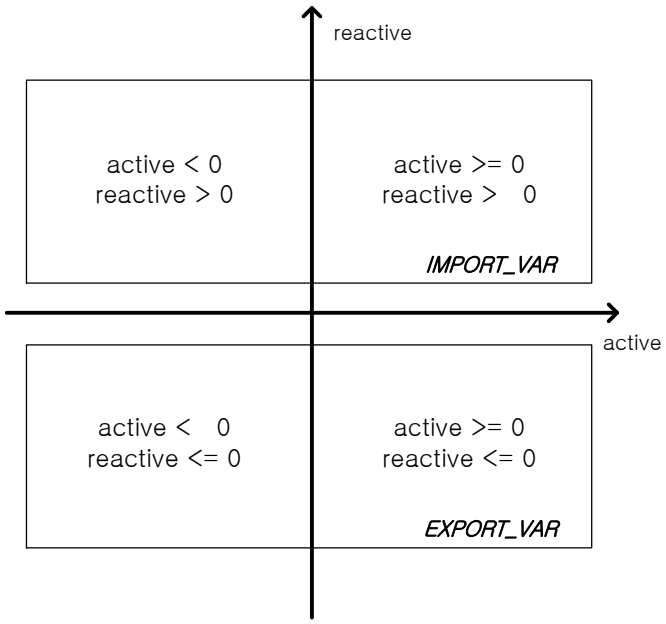


Figure 17-3 Deriving of reactive energy (REACT_SEL=0)

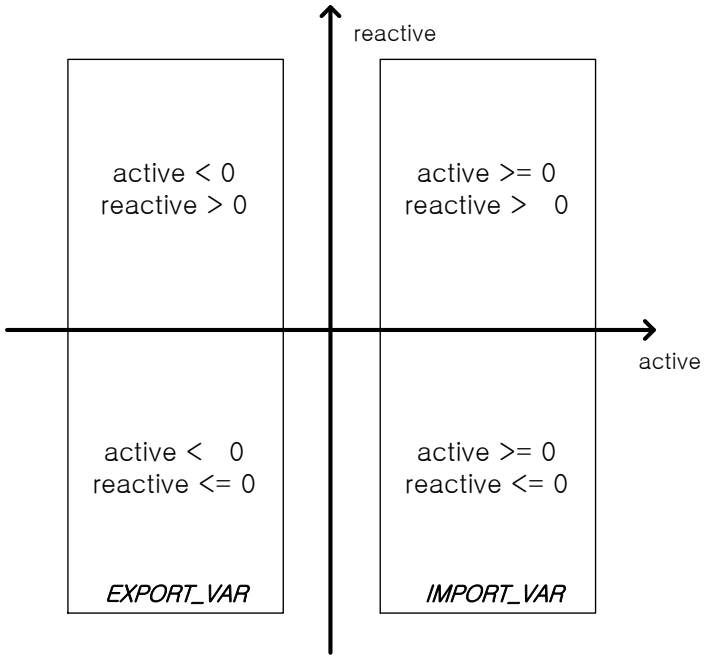


Figure 17-4 Deriving of reactive energy (REACT_SEL=1)

The output pulse is generated at a rate proportional to each power amount. SEM8310S generates 10 different output pulses simultaneously and has 2 pulse output pins. Figure 17-5 shows the operation of the pulse output multiplexer. The PULSE_OUT_SEL1 [3: 0] register determines the energy pulse to be connected to LED port 1 and the PULSE_OUT_SEL2 [3: 0] register determines the energy pulse to be connected to LED port 2 do. Table 17.4-2 shows the amount of power output to the LED port according to the setting values of the PULSE_OUT_SEL1 and PULSE_OUT_SEL2 registers.

Table 17.4-2 PULSE_OUT_SEL1/PULSE_OUT_SEL2 Register

PULSE_OUT_SEL1/PULSE_OUT_SEL2	Energy quantity connected to LED port
0	IMPORT_WH
1	EXPORT_WH
2	VAH
3	IMPORT_VARH
4	EXPORT_VARH
5	IMPORT_LAG_VARH
6	IMPORT_LEAD_VARH
7	Not used
8	EXPORT_LEAD_VARH
9	EXT_ENERGY1
10	EXPORT_LAG_VARH

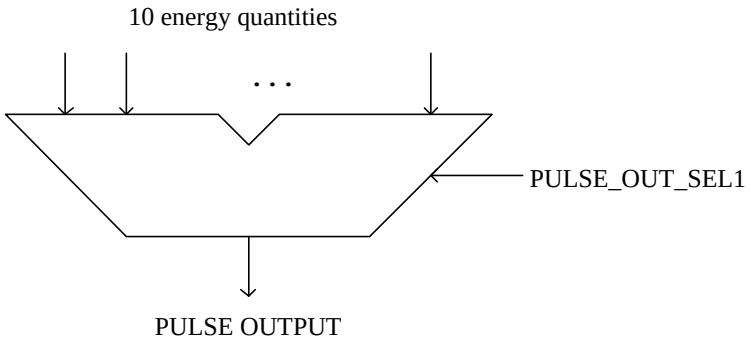


Figure 17-5 Pulse LED output MUX

17.5 Relationship between LED pulse on duration and power

The SEM8310S simultaneously generates the numerical power value and the pulse output signal. The period of the output pulse is determined by the DFC_GAIN register, which is determined in proportion to the meter constant of the watt-hour meter, and the lighting duration of the output pulse is determined by the DFC_DUTY register. Table 17.5-1 shows the unit output pulse lighting duration time when DFC_DUTY = 1 according to the setting value of EMB_OP [10] register.

Table 17.5-1 Unit pulse duration

EMB_OP[10]	Pulse light-on duration(DFC_DUTY=1)
0(31250Hz)	32us
1(125000Hz)	8us

Figure 17-6 shows the relation between pulse output and corresponding power quantity register. The power quantity register is incremented by the instrument constant K / 100 for one pulse output.

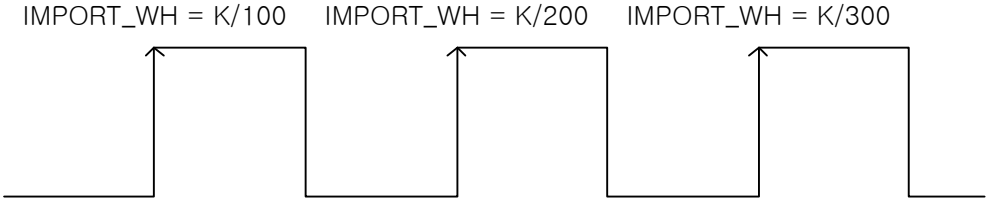


Figure 17-6 Relationship between pulse output and energy regisister

17.6 SAG/SWELL detection

Address	***Bit***	***Register***	***Description***	***Default***	***R/W***
0x8002_2078	12	SAG_THR	Sag detection threshold	0x22A	R/W
0x8002_207C	16	SWELL_THR	Swell detection threshold	0x33F	R/W
0x8002_20A0	2	SAG_STAT	SAG status for three input voltage SAG_STAT[1] : Sag SAG_STAT[0] : Swell	-	R
0x8002_20A4	27	SAG_ACC	The absolute value of the half-cycle accumulation value	-	R

The SEM8310S has a dedicated SAG / Swell detection block to detect instantaneous voltage sags and swells. Directly use the gain-compensated ADC output to detect voltage drop and rise quickly. Figure 17 10 Power Fail Indicates the I / O signal of the detection

block.

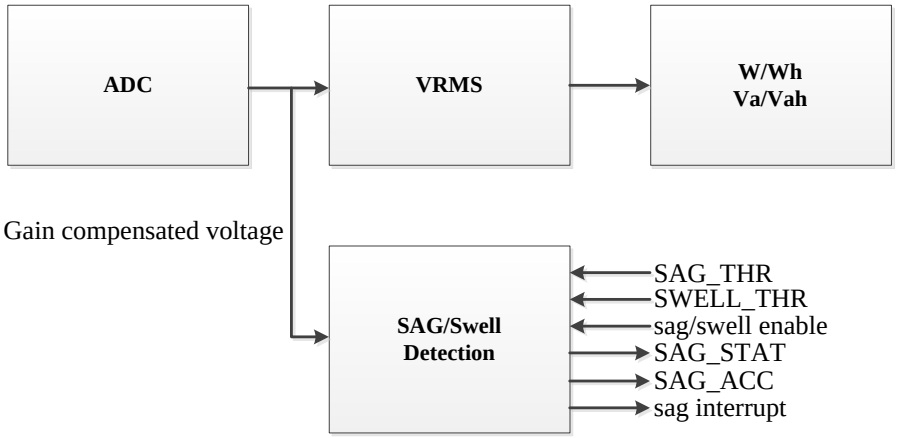


Figure 17-7 Sag / Swell detector block diagram

Figure 17 shows the Sag / Swell detection waveform. The SAG_ACC register compensates the gain of the voltage ADC output of each phase and accumulates it by half a period. If the upper 12 bits of these values are smaller than the value set in the SAG_THR register or greater than the value set in the SWELL_THR register, a SAG interrupt occurs. Then, it indicates to SAG_STAT register which interrupt in each phase. In addition, the ADC output value with gain compensation is cumulatively detected every half period, so that SAG / Swell occurs and it can be detected within half a period.

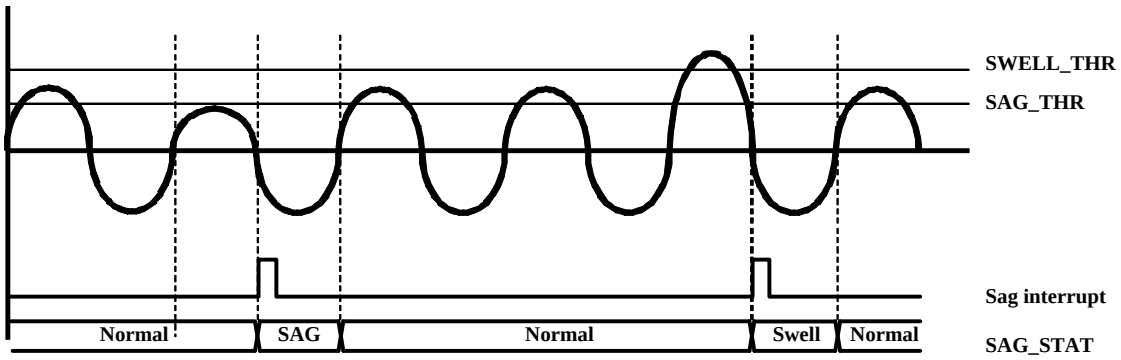


Figure 17-8 Sag/Swell detection waveform

17.7 Power Fail detection

Address	*Bit*	*Register*	*Description*	*Default*	*R/W*
0x8002_2070	21	PFAIL_THR	Power fail threshold	0x2932E0	R/W
0x8002_2074	15	PFAIL_DUR	Power fail duration	0xFA0	R/W
0x8002_209C	3	PFAIL_STAT	Power fail status for three input voltage PFAIL_STAT[0] : Power fail	-	R

If the VRMS value falls below a certain level (PFAIL_DUR) or below a certain level (PFAIL_THR) defined by the firmware, as shown in Figure 17.9, the PFAIL interrupt is generated. The PFAIL_DUR register is the number of ADC samples. The voltage imaging is detected using the VRMS value as shown in Figure 17 10, and a delay of about 150 ms,

which is the VRMS operation delay time, occurs until voltage imaging occurs and is detected.

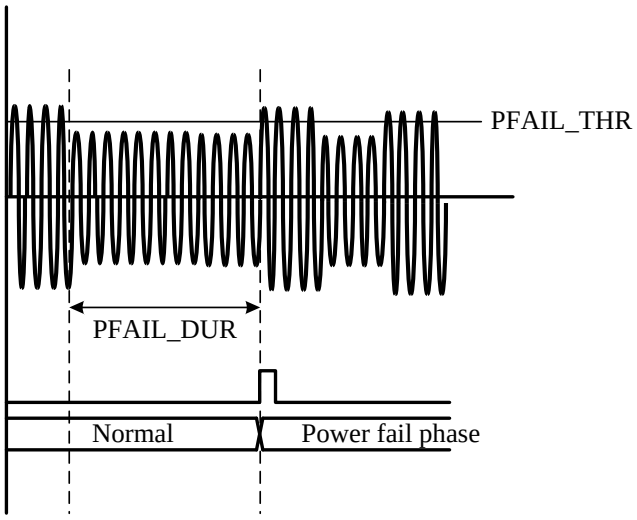


Figure 17-9 Power Fail detection waveform

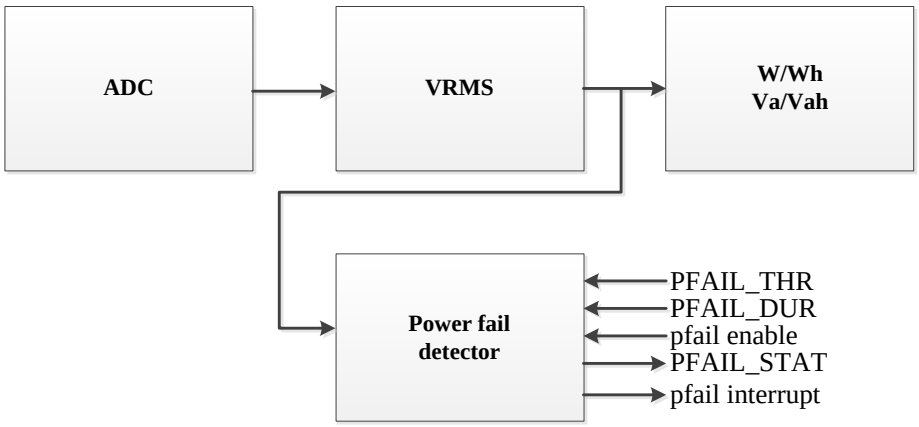


Figure 17-10 Power Fail Detection Block

17.8 EMB reset register

Address	*Bit*	*Register*	*Description*	*Default*	*R/W*
0x8002_2174	1	EMB_RESET_MODE	EMB reset mode 0 : Normal reset 1 : reset without EMB	0	R/W

The EMB_RESET_MODE register is used to set whether to reset the EMB when the

SEM8310S is reset. If EMB_RESET_MODE register is 0, EMB is reset when SEM8310S is reset. If SEM8310S is reset, EMB is not reset and retains the previous value when SEM8310S is reset. This is because EMB is not reset even if MCU part is reset after updating the firmware in firmware update.

18 LCD CONTROLLER

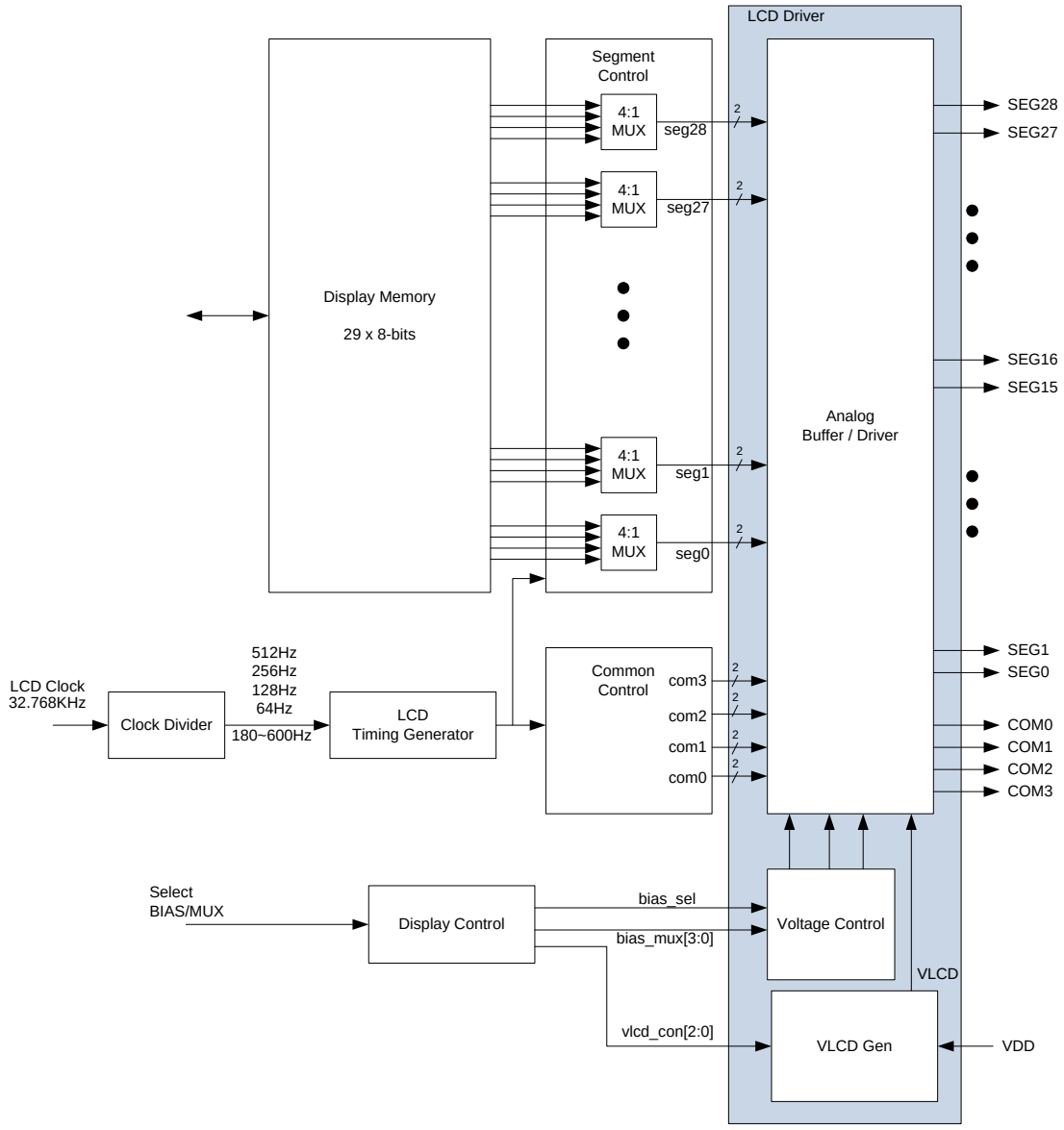
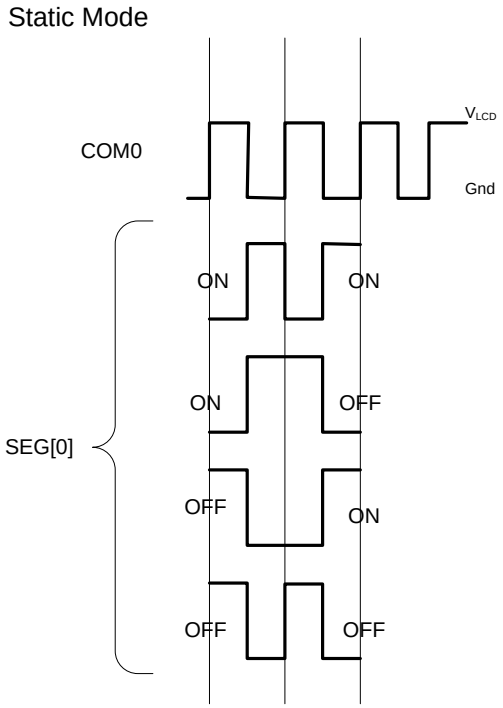


Figure 18-1 LCD Controller Block Diagram

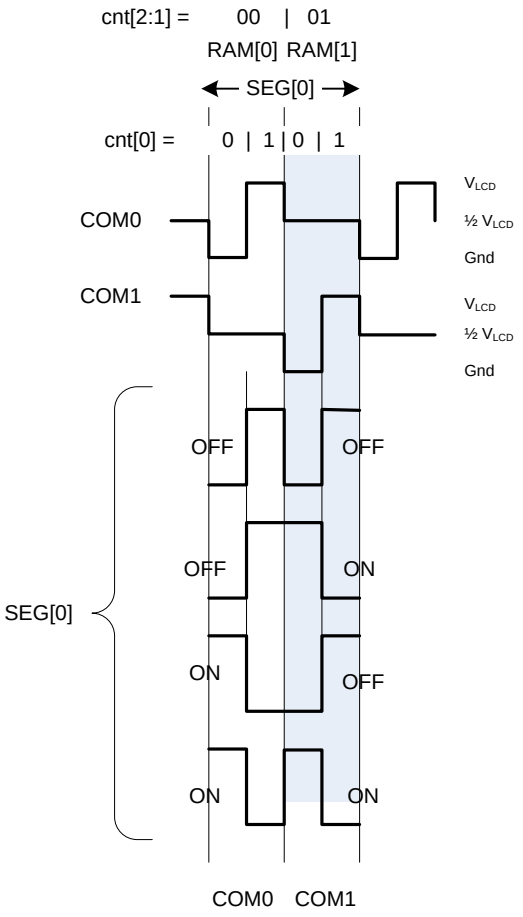
18.1 Timing Generator Timing Diagram

18.1.1 Static Mode



18.1.2 1/2 Bias and 2 COMs

2-Mux Mode ½ BIAS

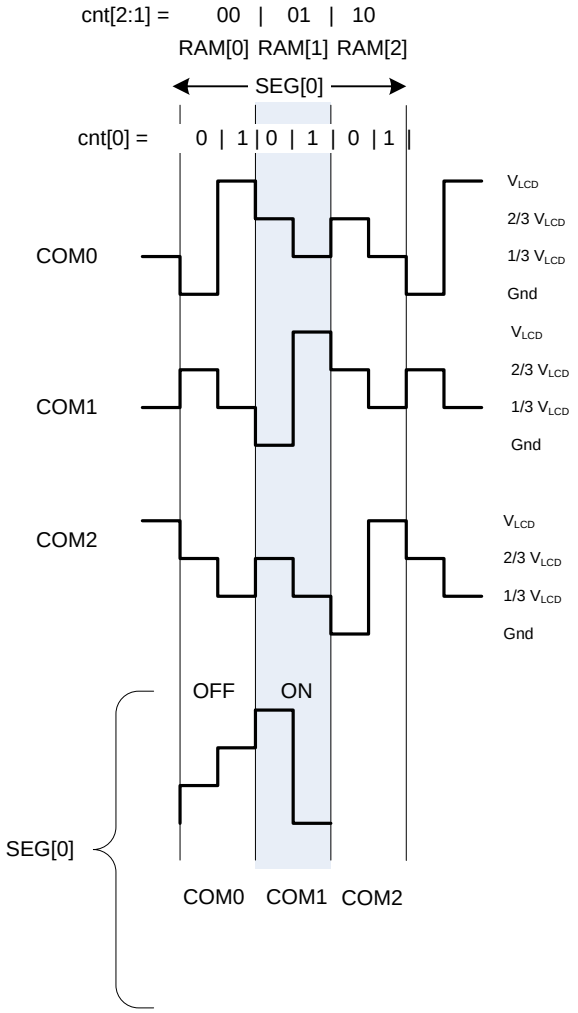


[Note] Multi-level voltage representation

: V_{LCD} = 2'b11, (V_{LCD} + V_{SS})/2 = 2'b10, V_{SS} = 2'b00

18.1.3 1/3 Bias and 3 COMs

3-Mux Mode 1/3 BIAS

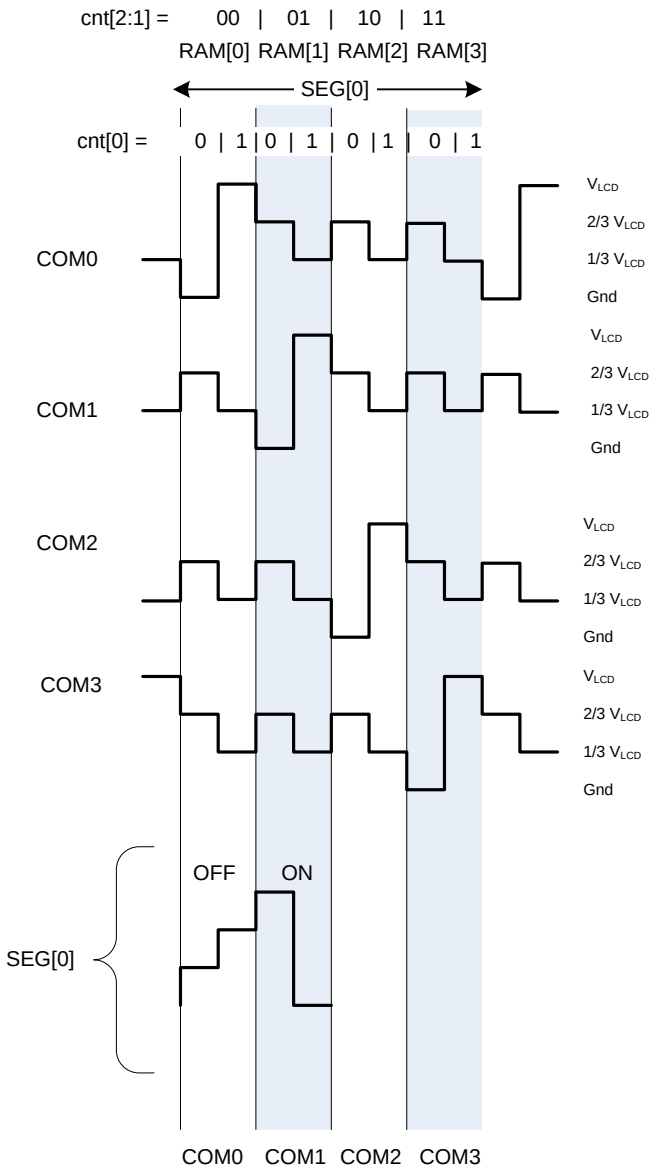


[Note] Multi-level voltage representation

: V_{LCD} = 2'b11, V_2 = 2'b10, V_1 = 2'b01, V_{SS} = 2'b00

18.1.4 1/3 Bias and 4 COMs

4-Mux Mode 1/3 BIAS



[Note] Multi-level voltage representation

: V_{LCD} = 2'b11, V_2 = 2'b10, V_1 = 2'b01, V_{SS} = 2'b00

18.2 LCD Control Registers

LCD Control Register (LCDCTRL)

Address : 0x8002_2400

Bit	R/W	Description	Default Value
31 : 18	R	Reserved	-
17 : 16	R/W	Clock Selection 00 : 64Hz 01 : 128Hz 10 : 256Hz 11 : 512Hz	00
15	R	Reserved	-
14 : 12	R/W	VLCD con 000 : 001 : 010 : 011 : 100 : 101 : 110 : 111 :	
11 : 10	R	Reserved	-
9 : 8	R/W	LCD common select bit 00 : Static 01 : 2 common 10 : 3 common 11 : 4 common	11
7 : 5	R	Reserved	-
4	R/W	LCD bias select bit 0 : 1/3 bias 1 : 1/2 bias	0
3 : 2	R	Reserved	-
1	R/W	Power Enable 0 : Disable 1 : Enable	0
0	R/W	LCD enable bit 0 : Disable 1 : Enable	0

LCD Control Register2 (LCDCTRL2)

Address : 0x8002_2404

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15	R/W	LCD Driver Test Enable 0 : Disable 1 : Enable	0
14 : 12	R	Reserved	-
11 : 8	R/W	LCD BIAS[3:0]	0000b
7 : 1	R	Reserved	-
0	R/W	LCD seg on 0 : Disable 1 : Enable	1

LCD RAM Data 0 Register (LCDDAT0)

Address : 0x8002_2410

SEG	Bit	R/W	Description				Default Value
			COM3	COM2	COM1	COM0	
SEG7	31 : 28	R/W	3f	3g	3e	DP	0
SEG6	27 : 24	R/W	2a	2b	2c	2d	0
SEG5	23 : 20	R/W	2f	2g	2e	Error	0
SEG4	19 : 16	R/W	1a	1b	1c	1d	0
SEG3	15 : 12	R/W	1f	1g	1e	T2	0
SEG2	11 : 8	R/W	S5	S1	S2	T1	0
SEG1	7 : 4	R/W	T3	S4	S3	T4	0
SEG0	3 : 0	R/W	A1	B	C	D	0

* See Figure 18-2 for the meaning of each SEG.

LCD RAM Data 1 Register (LCDDAT1)

Address : 0x8002_2414

SEG	Bit	R/W	Description				Default Value
			COM3	COM2	COM1	COM0	
SEG15	31 : 28	R/W	6a	6b	6c	6d	0
SEG14	27 : 24	R/W	6f	6g	6e	DP2	0
SEG13	23 : 20	R/W	5a	5b	5c	5d	0
SEG12	19 : 16	R/W	5f	5g	5e	○	0
SEG11	15 : 12	R/W	MEM	COL1	DP1	LOAD	0
SEG10	11 : 8	R/W	4a	4b	4c	4d	0
SEG9	7 : 4	R/W	4f	4g	4e	TEST	0
SEG8	3 : 0	R/W	3a	3b	3c	3d	0

* See Figure 18-2 for the meaning of each SEG.

LCD RAM Data 2 Register (LCDDAT2)

Address : 0x8002_2418

SEG	Bit	R/W	Description				Default Value
			COM3	COM2	COM1	COM0	
SEG23	31 : 28	R/W	S11	S10	S9	×	0
SEG22	27 : 24	R/W	S8	z	h	r	0
SEG21	23 : 20	R/W	k	V1	V2	A2	0
SEG20	19 : 16	R/W	8a	8b	8c	8d	0
SEG19	15 : 12	R/W	8f	8g	8e	DP4	0
SEG18	11 : 8	R/W	7a	7b	7c	7d	0
SEG17	7 : 4	R/W	7f	7g	7e	DP3	0
SEG16	3 : 0	R/W	BAT	S6	S7	COL2	0

* See Figure 18-2 for the meaning of each SEG.

LCD RAM Data 3 Register (LCDDAT3)

Address : 0x8002_241C

SEG	Bit	R/W	Description				Default Value
			COM3	COM2	COM1	COM0	
	31 : 28	R/W	Reserved				0
	27 : 24	R/W	Reserved				0
	23 : 20	R/W	Reserved				0
	19 : 16	R/W	Reserved				0
SEG27	15 : 12	R/W					0
SEG26	11 : 8	R/W					0
SEG25	7 : 4	R/W					0
SEG24	3 : 0	R/W					0

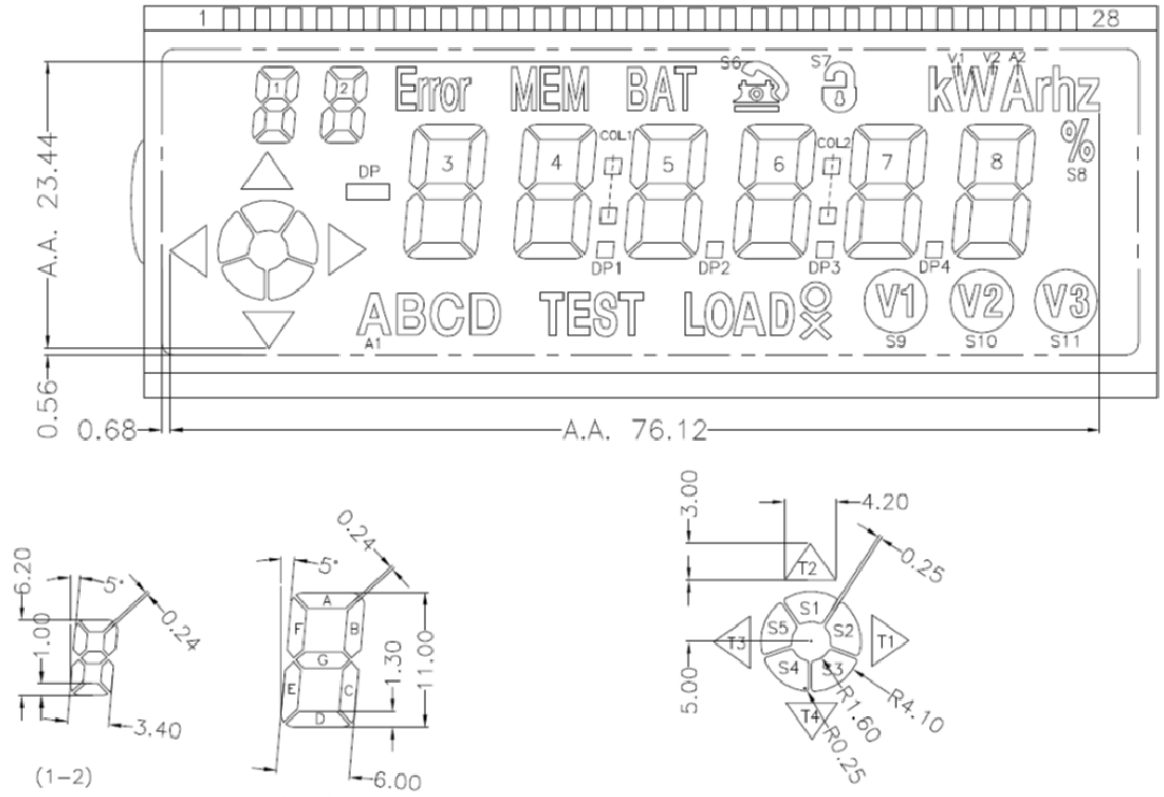


Figure 18-2 LCD Mapping Information

19 PIN ALTERNATE FUNCTION

19.1 Pin Alternate Function Registers

Pin Alternate Function 0 Register (PAF0)

Address : 0x8002_3C00

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 14	R/W	P0.7 : P0.7 Pin selection bit 0 : KEY_O[1] 1 : SLDI 2 : Reserved 3 : GPIO PA[7]	3
13 :12	R/W	P0.6 : P0.6 Pin selection bit 0 : EIRQ[2] 1 : RXD[0] 2 : Reserved 3 : GPIO PA[6]	3
11 : 10	R/W	P0.5 : P0.5 Pin selection bit 0 : EIRQ[1] 1 : TXD[0] 2 : Reserved 3 : GPIO PA[5]	3
9 : 8	R/W	P0.4 : P0.4 Pin selection bit 0 : MUX_SYNC 1 : EIRQ[0] 2 : Reserved 3 : GPIO PA[4]	3
7 : 6	R/W	P0.3 : P0.3 Pin selection bit 0 : RXD[1] 1 : SPI_nSS 2 : Reserved 3 : GPIO PA[3]	3
5 : 4	R/W	P0.2 : P0.2 Pin selection bit 0 : TXD[1] 1 : SPI_SCK 2 : Reserved 3 : GPIO PA[2]	3
3 : 2	R/W	P0.1 : P0.1 Pin selection bit 0 : Reserved 1 : SPI_MISO 2 : Reserved 3 : GPIO PA[1]	3
1 : 0	R/W	P0.0 : P0.0 Pin selection bit 0 : Reserved 1 : SPI_MOSI 2 : Reserved 3 : GPIO PA[0]	3

*** P0.0 ~ P0.3 Pin is set to Digital function or Analog Pin according to AFSR (0x8002_3C0C) setting. When analog function is set, P0.0 ~ P0.3 can not be used

Pin Alternate Function 1 Register (PAF1)

Address : 0x8002_3C04

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 14	R/W	P1.7 : P1.7 Pin selection bit 0 : TXD[2] 1 : PO_REACT 2 : PO_ACT 3 : GPIO PB[7]	3
13 :12	R/W	P1.6 : P1.6 Pin selection bit 0 : PO_REACT 1 : Reserved 2 : Reserved 3 : GPIO PB[6]	3
11 : 10	R/W	P1.5 : P1.5 Pin selection bit 0 : PO_ACT 1 : Reserved 2 : Reserved 3 : GPIO PB[5]	3
9 : 8	R/W	P1.4 : P1.4 Pin selection bit 0 : TWI_SCL 1 : Reserved 2 : Reserved 3 : GPIO PB[4]	3
7 : 6	R/W	P1.3 : P1.3 Pin selection bit 0 : TWI_SDA 1 : Reserved 2 : Reserved 3 : GPIO PB[3]	3
5 : 4	R/W	P1.2 : P1.2 Pin selection bit 0 : KEY_I[0] 1 : SLENB 2 : Reserved 3 : GPIO PB[2]	3
3 : 2	R/W	P1.1 : P1.1 Pin selection bit 0 : KEY_I[1] 1 : SLCLK 2 : Reserved 3 : GPIO PB[1]	3
1 : 0	R/W	P1.0 : P1.0 Pin selection bit 0 : KEY_O[0] 1 : SLDO 2 : Reserved 3 : GPIO PB[0]	3

Pin Alternate Function 2 Register (PAF2)

Address : 0x8002_3C08

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
3 : 2	R/W	P2.1 : P2.1 Pin selection bit 0 : PO_ACT 1 : PO_REACT 2 : Reserved 3 : PC[1]	3
1 : 0	R/W	P2.0 : P2.0 Pin selection bit 0 : RXD[2] 1 : Reserved 2 : Reserved 3 : PC[0]	3

Analog Function Selection Register (AFSR)

Address : 0x8002_3C0C

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
3	R/W	AF3 : Analog Function 3 selection bit 0 : PAF0.3 1 : LCD_SEG[27]	0
2	R/W	AF2 : Analog Function 2 selection bit 0 : PAF0.2 1 : LCD_SEG[26]	0
1	R/W	AF1 : Analog Function 1 selection bit 0 : PAF0.1 1 : LCD_SEG[25]	0
0	R/W	AF0 : Analog Function 0 selection bit 0 : PAF0.0 1 : LCD_SEG[24]	0

20 ELECTRICAL CHARACTERISTICS

20.1 DC Electrical Characteristics

Table 20.1-1 DC Electrical Characteristics

Parameter		*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Unit*
I/O Supply Voltage		DVDD		3.0	3.3	3.6	V
Junction Temperature		T_J		-40	25	125	°C
Operation Temperature		T_A		-40	25	85	°C
Input Low Voltage		V_{IL}		-0.5		0.8	V
Input High Voltage		V_{IH}		2.0		5.5	V
Schmitt Trigger Hysteresis		V_{HYS}		0.34	0.38	0.41	V
Input leakage current		I_I	VIN = VSS or 3.6V	–10		+10	uA
Input Current with Pull Down Resistor		I_{IL}	VIN = DVDD	+25	+58	+109	uA
Input Current with Pull Up Resistor		I_{IH}	VIN = 0	-26	-46	-74	uA
Output Low Voltage		V_{OL}		0		0.4	V
Output High Voltage		V_{OH}		2.4		3.6	V
MOSC Oscillator Frequency		f_{OSC}			16		MHz
ROSC Oscillator Frequency		f_{RTC}			32.768		KHz
Operating current	Run mode	I_{DD}	f_{SYSTEM} = 16MHz		29		mA
Deep Idle mode current		I_{DD}	f_{OSC} = Stop			150	uA

21 PACKAGE DIMENSION

Unit: mm

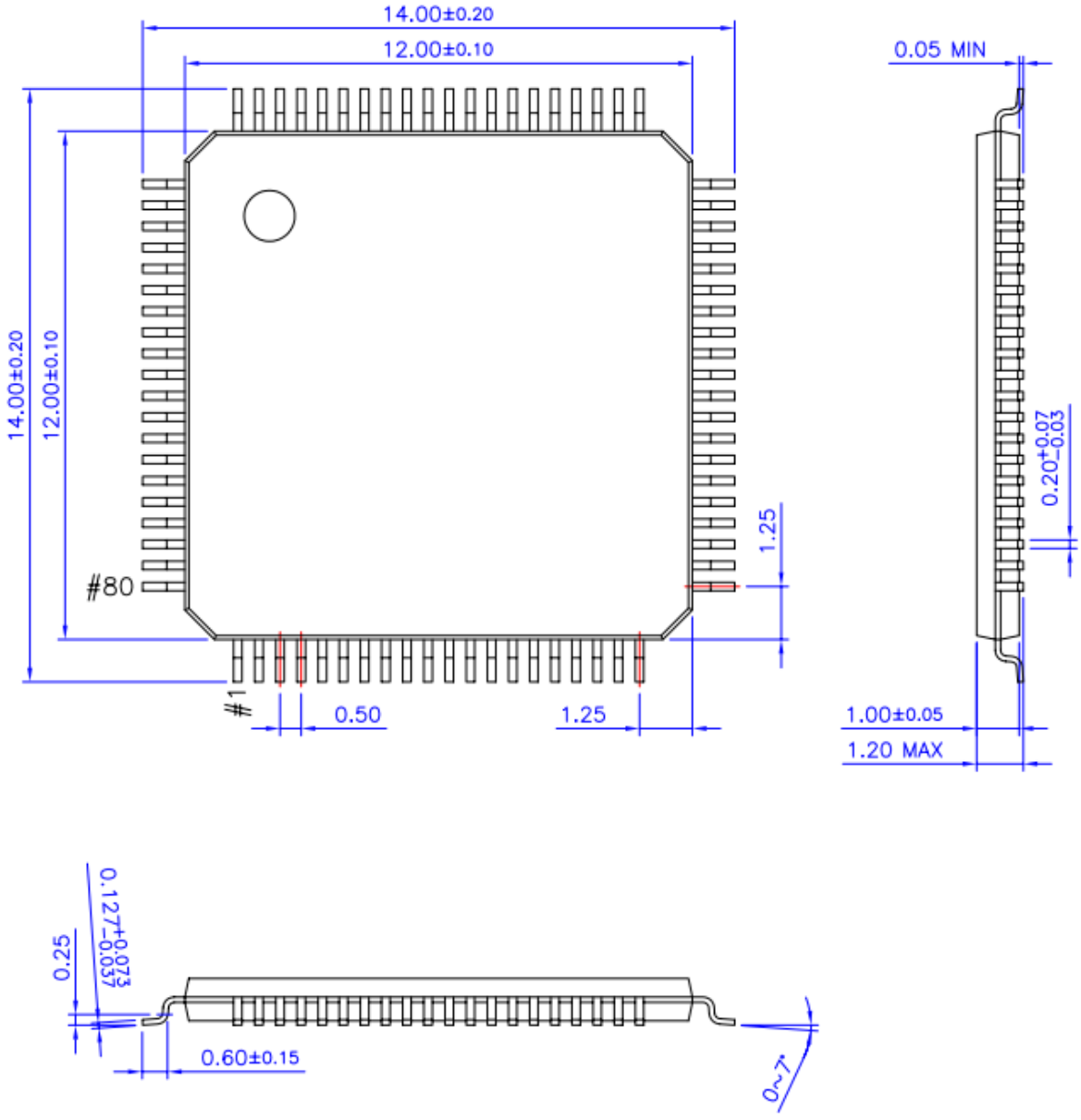


Figure 21-1 Package Drawing